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PHOTONIC HIGH-SPEED ANALOG-TO-DIGITAL SYSTEM TECHNOLOGY (PHAST)

ENSCO, Inc.

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PHOTONIC HIGH-SPEED ANALOG-TO-DIGITAL SYSTEM TECHNOLOGY (PHAST)

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13. ABSTRACT *(Maximum 200 words)*

The goal of the Photonic High-Speed Analog-to-Digital System Technology (PHAST) program was to develop a 10-bit, 10-Gsps analog-to-digital converter (ADC). This objective was to be accomplished in two phases: Phase I with a goal of delivering an 8-bit, 10-Gsps prototype system and Phase II which would focus on developing a 10-bit, 10-Gsps brassboard system. The basic approach uses filter elements to perform the processing required to establish the binary word output. The most promising method uses Mach-Zehnder interferometers as its key photonic processing component. Early in Phase I, a 4-bit ADC was fabricated and successfully tested. The 8-bit ADC required the development of a high-speed tunable laser, which was designed and in the process of fabrication when the project was unexpectedly cancelled by DARPA. This document details the progress and preliminary results in the development of the innovative high-speed, high-resolution analog-to-digital converter. It also describes the implementation plan and testing strategy that would have been used to provide the final system to meet the specified PACT program goals.

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Contents

Executive Summary

This document provides a comprehensive summary of the Photonic High-speed Analog-to-digital System Technology (PHAST) program and the results. PHAST supports the Photonic A/D Converter Technology (PACT) program of the Defense Advanced Research Projects Agency (DARPA). The goal of the PHAST program was to develop a 10-bit, 10-Gsps analog-to-digital converter (ADC). This objective was to be accomplished in two phases; Phase I with a goal of delivering an 8-bit, 10-Gsps prototype system, and Phase II, which would focus on developing a 10-bit, 10-Gsps brassboard system. Early in Phase I, a 4-bit ADC was fabricated and successfully tested. The 8-bit ADC required development of a high-speed tunable laser, which was designed and in the process of fabrication when the project was unexpectedly canceled by DARPA. At the time funding was cut, the percentage of technical completion was appropriate for the funding received. The existing design described in this document would have been used as the template to fabricate the Phase I prototype.

During the course of the project, the PHAST concept has evolved through several generations, each one resulting in significant improvement over the previous one. As a result, two competing approaches have emerged. The basic approach uses sophisticated filter elements to perform the processing required to establish the binary word output. The more promising approach, termed "the enhanced approach," uses Mach-Zehnder interferometers as its key photonic processing component. Exclusive use of Mach-Zehnder interferometers as the principle processing element for the enhanced approach supports an extremely high-speed system and efficient implementation because it relies on a mature and readily available technology. Both approaches require a tunable source as the key element. Development of this state-of-the-art source was in progress when funding was withdrawn and its preliminary design and simulation results are presented in this report. These results suggest that the tunable laser would not only have supported the PHAST ADC system goals, but also represented an extremely useful component in other areas, such as Wavelength Division Multiplexing (WDM) networking applications. The innovative nature and involved fabrication schedule of this device added an element of risk to the project, but because of the tremendous impact that this component would have towards this and other Department of Defense (DoD) applications, we enthusiastically pursued its development.

To validate and evaluate the PHAST concepts, a build plan and schedule were formulated and are detailed in this document. Before project cancellation, the build plan was the strategy to allow the PHAST team to efficiently meet the goals of the PHAST Phase I effort; that is, to design, assemble, and test a working 8-bit, 10-Gsps-prototype system. By employing several build phases, we optimized the likelihood of meeting the project goals.

In summary, this document details the progress and preliminary results in the development of an innovative high-speed, high-resolution analog-to-digital converter. It also describes the implementation plan and testing strategy that would have been used to provide the final system to meet the specified PACT program goals.

PHAST Final Report

1 Introduction

This document provides a comprehensive summary of the Photonic High-speed Analog-to-digital System Technology (PHAST) program and the results. PHAST supports the Photonic A/D Converter Technology (PACT) program of the Defense Advanced Research Projects Agency (DARPA). The goal of the PHAST program was to develop a 10-bit, 10-Gsps analog-to-digital converter (ADC). This objective was to be accomplished in two phases; Phase I with a goal of delivering an 8-bit, 10-Gsps prototype system, and Phase II, which would focus on developing a 10-bit, 10-Gsps brassboard system. Early in Phase I, a 4-bit ADC was fabricated and successfully tested. The 8-bit ADC required development of a high-speed tunable laser, which was designed and in the process of fabrication when we were redirected to stop work on the project. The existing design described in this document would have been used as the template to fabricate the Phase I prototype.

Early in the effort, it became apparent that a high-speed tunable laser would have to be designed as the critical part of the project, even though laser development is not specified in the statement of work (SOW) for Phase I. We were directed to focus on the laser development, rather than the completion of the 8-bit ADC. At project reviews, including the DARPA/MTO 2000 Optoelectronics Review in Cincinnati, OH, 18 October 2000, representatives from both the Air Force Research Laboratory (AFRL) and DARPA stated that the project goal should be the demonstration of a successful laser. AFRL and DARPA emphasized that the processor portion of the ADC was not only a secondary issue, but also not very useful unless the tunable source could be demonstrated. Also, part of the processor operation requirements could only be specified once the tunable laser characteristics were known. We were consequently directed to make the laser fabrication and demonstration our top priority. The laser had been designed and simulated using the Photonic Transmission Design Suite (PTDS) from Virtual Photonics, and the semiconductor mask and wafer had been designed and ordered. The only remaining activities were the fabrication and testing of the laser. All other tasks, except those related to the 8-bit ADC Processor development, had been completed at the time we were redirected to stop work. This document describes the completed portion of the contract and indicates the schedule that would have been followed for full completion.

This document contains seven technical sections. The first, Section 2, provides a technical overview and description of the operation and analysis of the predicted performance of the PHAST system. This section provides analytic data and simulation results indicating that the system could achieve the overall stated goals of this effort. The components of the PHAST system are described in detail in Sections 3 through 7. A discussion of the operation of the processor portion of the basic PHAST system is in Section 3. Section 4 presents a detailed survey of the likely candidates for the processor filters. Section 5 gives an overview of the principles used to design the tunable sources for the ADC application and describes the basic laser approach in some detail. Also discussed in Section 5 is the improved tunable laser that includes a second Fabry-Perot filter. Research conducted by the PHAST team, as detailed in Section 6, shows that a tunable laser system with speed and resolution requirements compatible

with this effort is possible. This section also provides simulation results for this enhanced tunable laser system. Section 7 provides the design and fabrication details for the laser. Section 8 gives the plan for the integrated tunable laser build and the schedule that would have been used for the development and evaluation of the proof-of-concept devices and breadboard system, as well as the final prototype system. This section shows the methods used to minimize the risk of achieving the Phase I goal of an 8-bit, 10-Gsps system.

2 PHAST System Technical Overview

During the course of the project, the PHAST concept has evolved through several generations, with each one resulting in significant improvement over the previous one. Two complementary approaches have emerged as a result of this research. The basic approach, as will be described, uses passive filters working in conjunction with a tunable source to establish the binary word output. A more promising approach under development, termed "the enhanced PHAST system," uses Mach-Zehnder interferometers as its key processing component. These Mach-Zehnder interferometers provide a folding and linearization capability, described later in this section. Use of Mach-Zehnder interferometers as the principle processing element supports an extremely fast system that relies on a mature and readily available technology. Both of these system approaches use a tunable laser as a major component. Details of the two systems will be presented in the remainder of this section. We first start with a discussion of the basic PHAST system approach with emphasis on the understanding of the underlying concepts, followed by a detailed description of the current design approach.

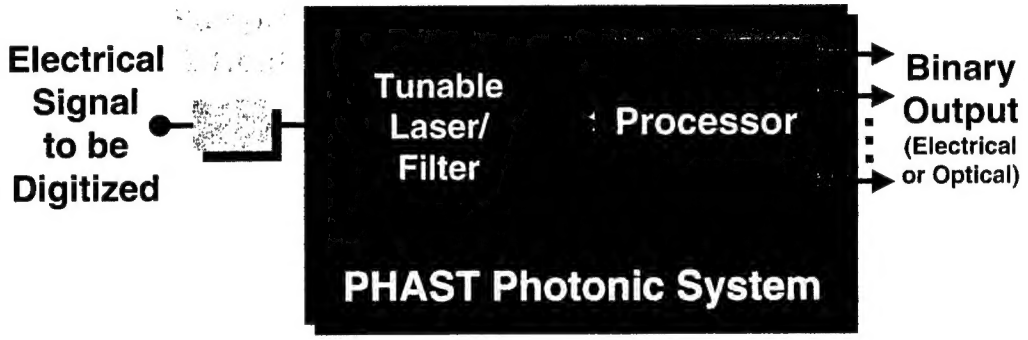

Figure 1. Basic PHAST system block diagram.

2.1 Technical Background

This technical overview begins by reviewing the fundamental concepts that govern the operation of the PHAST tunable wavelength-based all-photonic ADC converter. The basic (i.e., the original) approach for an all-optical ADC is illustrated in Figure 1, where it is seen that the photonic portion of the system is composed of two major subsystems; a tunable wavelength/frequency source, and the corresponding processor. The tunable source converts the input signal that is to be digitized to an optical frequency (or wavelength[1]) at its output, and can be thought of as a voltage controlled (optical) oscillator in which the information contained in the input voltage level is converted to a unique optical wavelength. The tunable source thus converts the ADC problem from one of resolving a voltage to one of resolving a wavelength (or wavelength band). The mapping between input voltage and optical frequency is ideally linear. If the relationship is other than linear, then either the input signal must be pre-conditioned to

[1] The system will function whether designed for linear tuning in frequency or wavelength, assuming that the processor is designed to map in a consistent way with the tunable laser approach selected. Most tunable laser and processor approaches naturally track linearly in frequency. To aide in clarity, optical signals in this document may be represented by either their optical frequency or wavelength equivalent, but for optimal performance, the laser and processor must be designed using a common mapping convention.

linearize the voltage to optical frequency conversion, or alternatively, the deviation from linearity must be accounted for in the design of the processor portion of the system. The processor represented in Figure 1 converts the optical frequency generated by the tunable source to the appropriate binary word.

2.1.1 Technical Overview of the Basic PHAST Approach

The basic PHAST system will now be examined in greater detail. For the purpose of this discussion, let us consider as an example the 4-bit ADC system, shown in Figure 2. The tunable source can be realized by either a tunable laser or the combination of a broadband source followed by a tunable filter. This voltage-encoded wavelength is split and directed to the bit-leg processor filters, where the correct binary digit is established. For example, suppose an input voltage level v_i tunes the source to wavelength λ_i, for which the desired binary word is $B_i = b_i^{MSB}$ b_i^{MSB-1} b_i^{LSB+1} b_i^{LSB}. Here, MSB is the most significant bit and LSB is the least significant bit. The processor filter would then be designed as follows. If the desired binary digit corresponds to a logical zero, then the wavelength transfer function of the bit-leg would prevent that wavelength from reaching the photodetector. Otherwise, that wavelength would be passed by the processor filter and detected as a logical one by the spectrally broad photodetector at the bit-leg output. For the purpose of this discussion, the filter transfer functions shown in Figure 2 are ideal. In practice, the combined effect of the finite transitions associated with realizable processor filters and the finite tunable source linewidth would have to be accounted for in the system design. This is done by the use of the electronic comparators also shown in the figure. Also included in the system are fixed delays to ensure that all bits have equal latency to avoid race conditions. A more detailed discussion of the operation of the processor portion of the basic PHAST system is given in Section 3. Section 4 presents a detailed survey of the likely candidates for the processor filters.

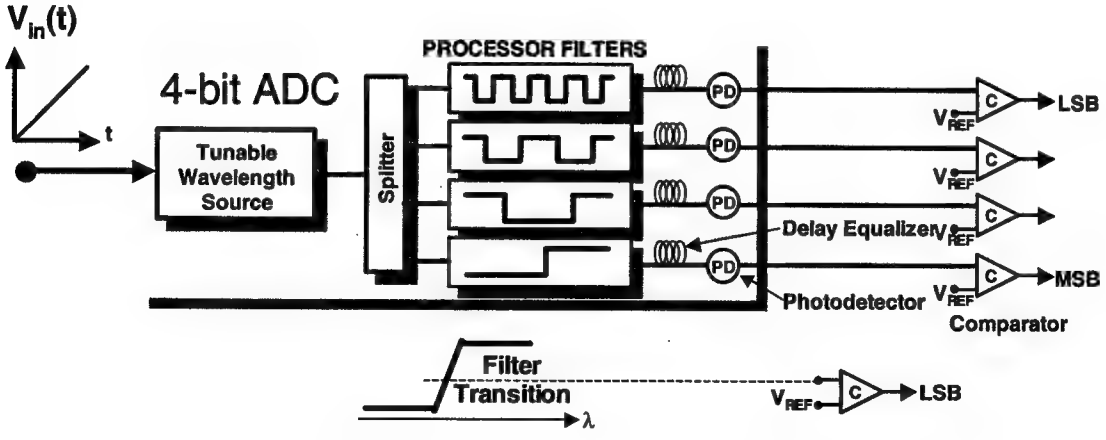

Figure 2. Basic PHAST approach showing idealized processor filter functions with electronic comparators at the output.

The above approach has several distinct advantages, including the potential for monolithic integration and an extremely simple architecture. The architecture has all passive

processing and tuning using a single control signal, hence negating the need for a slow look-up table and the electronics that would be associated with having to incorporate that capability. Note that a sample-and-hold capability is included in the previous figures. Although shown in the figures, DARPA has directed that the PHAST effort not pursue development of this component at this time and therefore, further discussion regarding the sample-and-hold will not appear in this document.

2.1.2 Limitations of the Basic Approach

One of the most difficult technical hurdles to realizing a high-speed, high-resolution ADC system, using the basic approach as described above, is the ability to generate the required number of distinct wavelengths at the desired speed. For example, assume an optimistic tuning range of $\Delta\lambda = 100$ nm. A 12-bit system would require a Finesse F of at least $F = 4096$ with a corresponding Free Spectral Range FSR of approximately $FSR = 3$ GHz (or $\Delta\lambda/4096 = 0.024$ nm). If this filtering function were performed by a Fabry-Perot resonant cavity, it would require a transit time τ of $1/2FSR = 163$ psec. If we approximate the number of cavity passes for convergence as being equivalent to the finesse, then the tuning time is found to be $\tau F = 669$ nsec, or a maximum tuning rate of about 1.5 MHz. This analysis ignores the gain in convergence speed that might be realized due to side-mode suppression resulting from the feedback in a laser configuration, as will be evident in the tunable laser section of this document. Even with the convergence speed improvement that might be provided by a tunable laser configuration, achieving the speed and resolution required for a 10-bit, 10-Gsps system is quite daunting. Nevertheless, research conducted by the PHAST team, as detailed in Section 6, shows that a tunable laser system with speed and resolution requirements compatible with this effort is possible. This goal is accomplished by means of an enhanced approach, one that uses amplitude as well as wavelength information and thus circumvents the speed-resolution bottleneck of the basic system is now be discussed in greater detail.

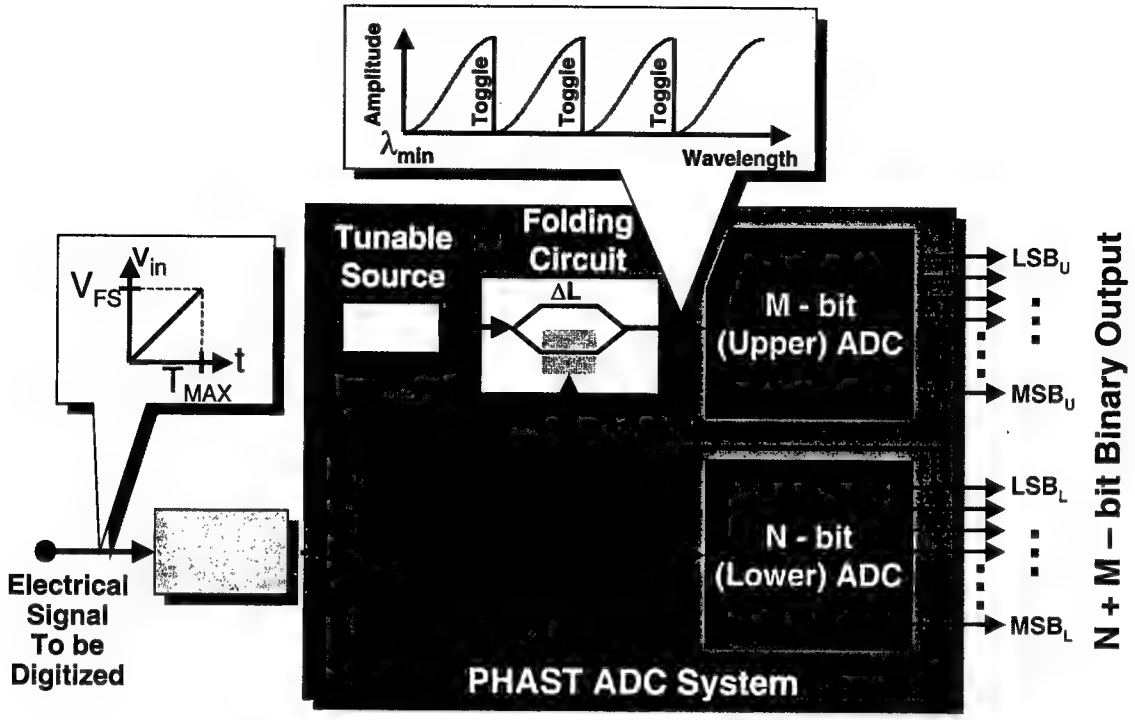

Figure 3. Enhanced system block diagram.

2.2 Enhanced PHAST System Approach Technical Overview

The previous discussion suggests that to achieve the goal of 10-Gsps tuning, the finesse of the (passive) tunable filter source must be reduced by roughly 3 orders of magnitude. Unfortunately, the reduction of the finesse would result in an unacceptable system resolution. In general, these requirements are incompatible with the basic PHAST approach. An enhanced approach, however, that does achieve the desired speed-resolution requirements has been devised. This approach uses two high-speed, reduced resolution ADCs, both working together in such a way that their concatenated outputs give the overall desired resolution. A block diagram of the enhanced approach is shown in Figure 3.

Specifically, Figure 3 shows two ADCs, the lower with N-bit resolution and the upper with M-bit resolution, coupled through a photonic folding circuit. The two lower resolution ADCs can be implemented using the basic PHAST photonic approach operating at a lower finesse. This lower finesse then allows operation at the desired speed.

2.2.1 The Basic Folding Circuit

With the aid of the folding circuit, the resolution of the composite system is *N+M*. This concept is illustrated in Figure 4 using idealized waveforms and, for the purpose of this discussion, assumes that the input voltage varies linearly between zero and its full-scale value (V_{FS}). To say that the resolution limit of the lower ADC system has been reached means that the linewidth of the tunable source, Figure 4A, and the width of the passband of the lower LSB (LSB_L) bit-leg filter, Figure 4B, are equal. The detected voltage, which is proportional to the integration of the product of the swept tunable source and LSB_L transfer function, is shown in

Figure 4C. The interesting consequence of this filtering-detection process is that, as the input voltage varies from zero to its full-scale value, not only is *all* its information still contained in the (appropriately conditioned) detected signal, but the periodic nature of this signal now allows the use of a second ADC to further resolve the input to a finer degree. This function is performed by the photonic subsystem referred to as the folding circuit.

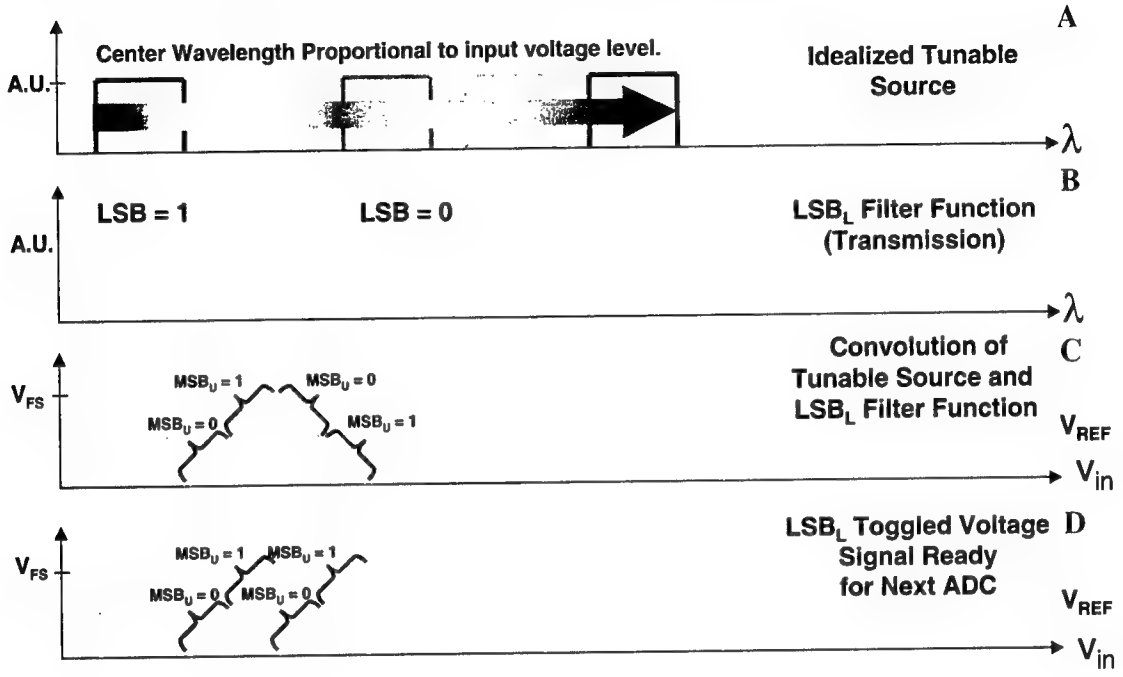

Figure 4. Operation of the folding circuit.

Now consider how additional information (bits) can be resolved from the output of the folding circuit. The triangular waveform of Figure 4C can be directly digitized by the upper ADC system. Because of the non-monotonic nature of the triangle waveform, we also considered an additional step that would "unwrap" the triangle wave and produce a sawtooth. This unwrapping is readily accomplished by incorporating a "toggle" capability as part of the folding circuit. Figure 4D shows how the LSB_L bit output acts as an appropriate toggle signal leading to a monotonic (ideally sawtooth type) response. This toggle can be accomplished in the folding circuit itself or in the digital regime. Referring back to Figure 3, however, it is seen that a practical folding circuit will result in waveforms that are nonlinear and that these nonlinearities must be corrected to extend the resolution of the upper ADC to more than one additional bit. As will be discussed, this linearization and toggle process are most efficiently accomplished together.

We later determined that the sawtooth was not as practical as the triangle waveform because of its discontinuous nature. However, our design was still specified in terms of the sawtooth waveform at the time we were redirected to stop work on the PHAST project, so the discussion in this document will be in terms of the sawtooth method. The discussion of how this linearization and other necessary signal conditioning is accomplished, along with the final ADC system design, is presented in the following section.

2.2.2 The Linearization Circuit

It was already noted that since the folding circuit is an interferometric system, the voltage output of the folding circuit does not vary linearly for a linearly increasing input signal. Specifically, the Mach-Zehnder output follows the distinctly nonlinear (approximately a raised cosine) curve shown in Figure 5A. When compared with the idealized linear signal desired (the dashed-curve shown in Figure 5A), we see that if we were to add an attenuated and phase-shifted version of this same signal to the original detected folding circuit output, then the deviation from linear would be substantially reduced. This transfer function must vary at twice the frequency of the folding Mach-Zehnder transfer function. This linearization is accomplished, as shown in Figure 6, by taking a portion (ε) of the optical output of the tunable source to feed another Mach-Zehnder filter. The Mach-Zehnder in the linearization circuit has a differential path length (ΔL) that is twice that of the folding Mach-Zehnder to achieve the required doubling in frequency. Due to the broadband nature of the source, the (uncorrected) folding circuit output is periodic, but not purely sinusoidal, hence it is not expected that a one-term correction would perfectly compensate the nonlinearity. This linearization process may be continued to yield higher-order correction terms. As will be seen in the next section, two levels of correction are generally not necessary, though one level is essential to resolve beyond a single additional bit.

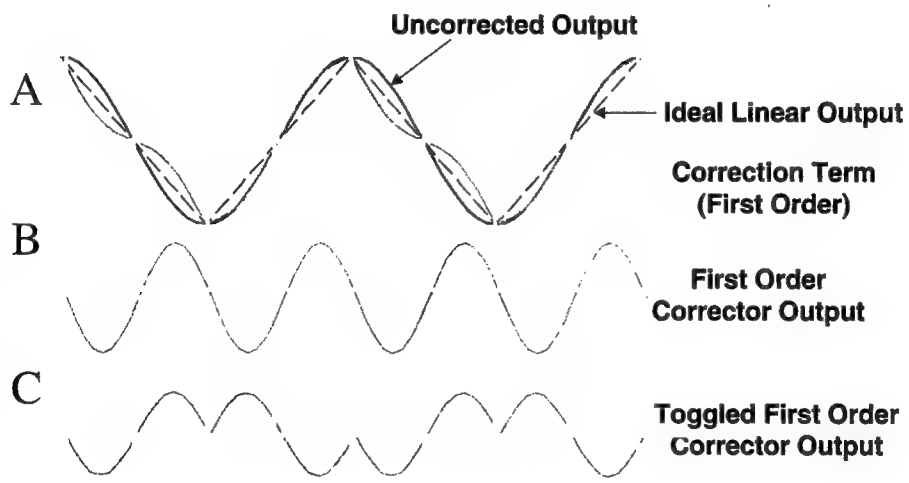

Figure 5. Nonlinear Mach-Zehnder response and correction term.

The reduced extinction ratio due to the finite linewidth source results in different dc levels for the detected correction and folding signals. To properly sum these signals, level shifting is required. DC level shifting, for example by using ac-coupled amplifiers, can be used to correct this situation.

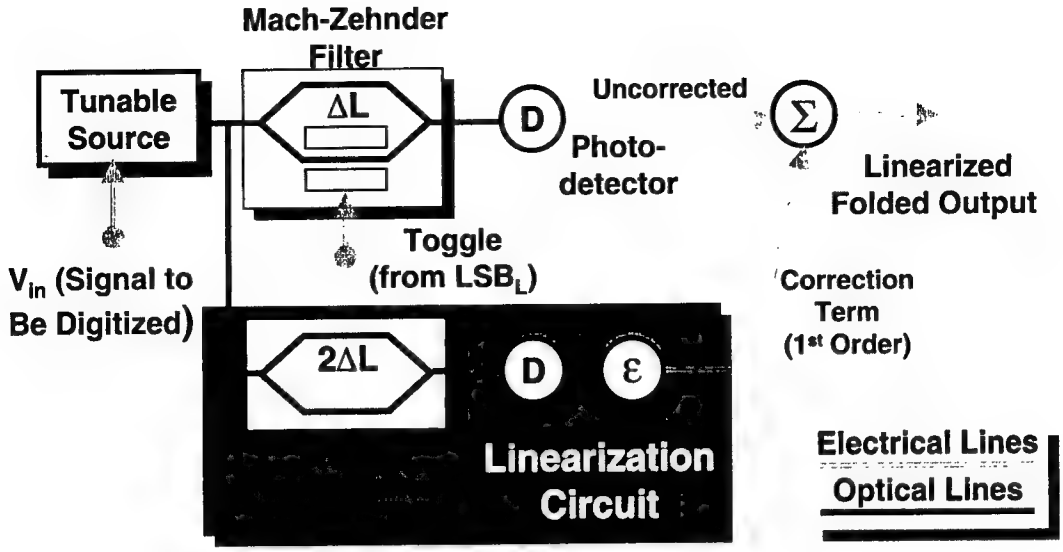

Figure 6. Linearization circuit.

An example of how the linearization circuit can significantly reduce nonlinearity, in the otherwise very non-linear response of the uncompensated folding circuit output, is illustrated with the aid of Figure 7. The upper set of curves in the figure compares the uncompensated detected signal (dashed curve) with that same signal plus a single linearization correction term. The impact of this linearization in the ADC resolution performance can be seen from the lower plot in the figure. This lower plot data indicates that the quantization error is reduced from less than eight system bits with no compensation to better than 10-bits and 11-bits for one and two linearization terms, respectively.

2.2.3 The Fully Functional Folding Circuit

At this point, we have discussed the two essential processing subsystems needed to implement the enhanced PHAST system. Additionally, an efficient, high-speed tunable source will be integrated with the folding and linearization circuits that together comprise the fully functional folding circuit.

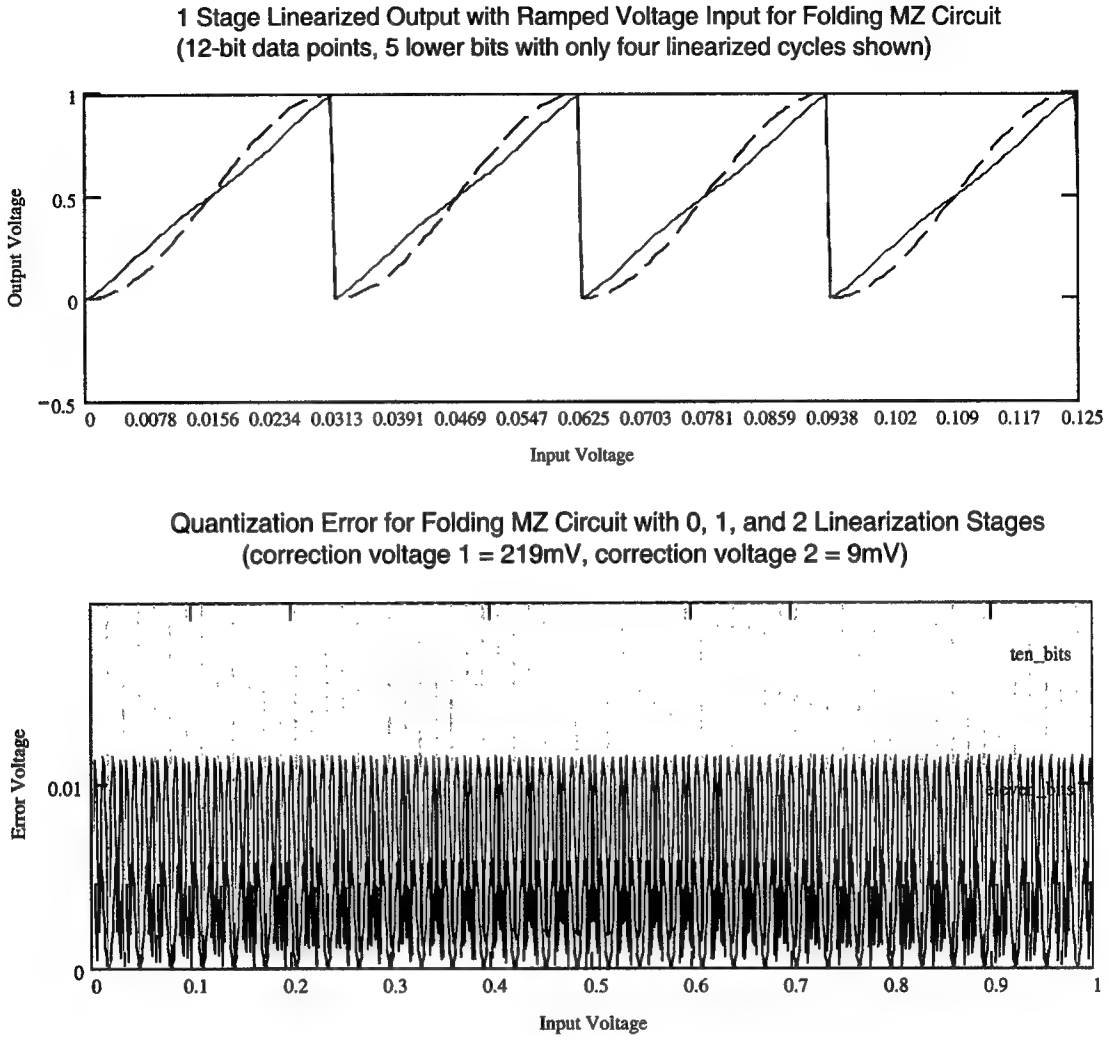

Figure 7. One and two term linearization system simulation results.

To use a lower ADC with N-bits of resolution requires a folding circuit that can produce an output with 2^N folds for any further increase in resolution for an upper ADC. Recall that each level of linearization contains a Mach-Zehnder with half the Free Spectral Range FSR_L of the previous level, or

$$FSR_L = \frac{FSR_P}{2^L},$$

where L is the level of linearization and FSR_P is the free spectral range of the folding Mach-Zehnder. Since 2^N folds are required over the free spectral range of the source FSR_S, and each cycle of the folding Mach-Zehnder produces two folds, then

$$FSR_P = \frac{FSR_S}{2^{N-1}}.$$

Since each linearization Mach-Zehnder has a finesse of two, its half-power bandwidth $HPBW_L$ is

$$HPBW_L = \frac{FSR_L}{2} = \frac{FSR_P}{2^{L+1}} = \frac{FSR_S}{2^{L+N}}.$$

The limit on the number of linearization terms L possible for a given source finesse is reached when the $HPBW_L = HPBW_S$, or

$$L = \log_2(F_S) - N.$$

Note that the ability to use linearization terms implies that sufficient source finesse is available to increase the number of folds in the processor Mach-Zehnder, and hence, based on this, the option exists to use a higher-resolution lower ADC. Of course, this option may not be possible based on the speed-resolution restrictions of the lower ADC.

2.3 Present PHAST System Design

This section summarizes the present design for the PHAST ADC system. Details are provided in the following sections. Note that state-of-the-art electronic ADCs can operate at speeds up to 20-Gsps at 6-bits of resolution, or 8-Gsps at 8-bit resolution. Electronic ADCs thus represent an efficient and mature technology. Our design takes full advantage of this technology by using two high-speed, lower resolution electronic ADCs to realize high-speed and high-resolution analog-to-digital conversion. Of course, it is required that these electronic ADCs, though operating at low resolution, will have a quantization error no greater than the desired total system resolution. The use of photonics for this ADC application thus allows two high-speed electronic ADCs to operate in unison in order to obtain the desired result. This idea is illustrated in Figure 8.

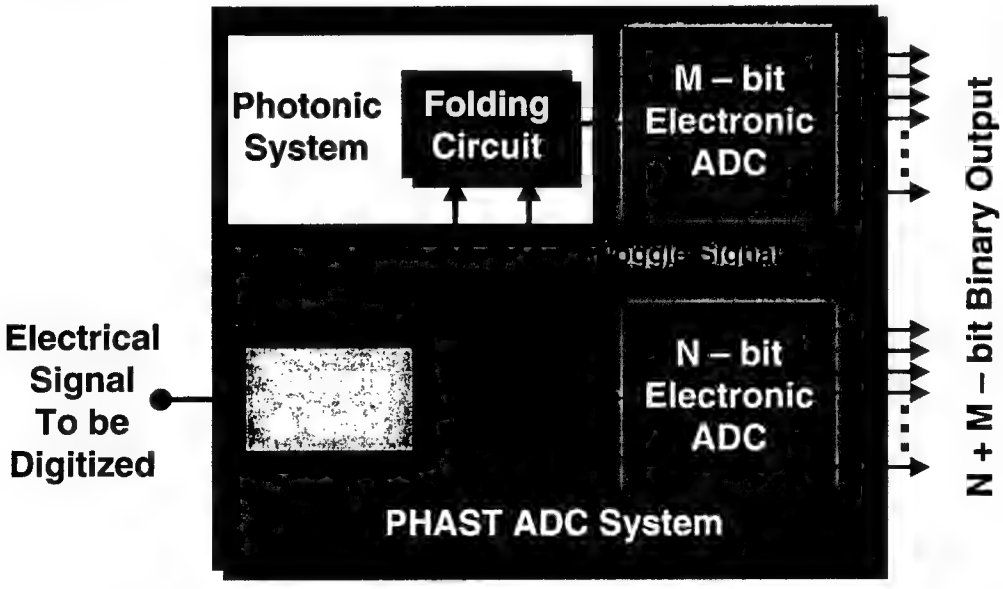

Figure 8. PHAST design.

The tunable laser system approach is closely related to the concept that was presented in Figure 3. Extensive modeling of the tunable laser has been performed. Initial results obtained from the models indicate the designs considered will achieve the desired tuning speed, with a wavelength resolution on the order of 6-bits. Adding a second tunable laser provides yet another bit of resolution with the remaining bits arising from the folded amplitude response that results from tuning the laser between lasing lines. These details are further described in Section 6.

3 PHAST Processor

This section provides an overview of the operation of the basic PHAST processor. As stated in Section 2, the purpose of processor is the mapping of the input wavelength, which corresponds to the voltage to be digitized, to the desired binary word at the output. As will be discussed, this mapping is accomplished by means of (passive) wavelength/frequency filtering. Although many approaches exist to realize these processor filters, as discussed in Section 4, the transfer function patterns required for each bit-leg filter as well as bit-leg to bit-leg filter relationships are the topic of this section.

3.1 Wavelength Encoding

To understand the basic processor operation and its requirements, consider as an example the logic table of a four-bit analog-to-digital converter shown in Table 1. First, note that in the table the 2^N=16 (N is the number of bits of resolution) discrete possible voltages to be digitized are represented by their corresponding wavelengths that would be output from the tunable laser. The second column and third column indicate the desired equivalent binary word for a standard mapping, as well as a Gray-coded mapping[2], respectively. Since rapid decoding is possible with post-detection logic, any coding scheme could be employed. However, to illustrate reduction in errors and system complexity, a Gray-coded mapping is provided as an example.

For the approach presented here, the optical signal from the tunable source is split N ways at the processor input and apportioned to each of the bit-legs as seen in Figure 9. Each of the N bit-legs will have its own filter element(s) whose overall transfer function corresponds to the pattern of 0s (logical zeros) and 1s (logical ones), as indicated in the columns for the binary count (or the Gray-coded binary count) in Table 1. These filter functions will block those wavelengths that are indicated by a logical zero, while those that correspond to a logical one are allowed to propagate with minimal loss to a spectrally broad (i.e. capable of detecting all wavelengths within the laser tuning range of interest) photo-detector. For example, for the MSB of the standard binary count approach, wavelengths λ_0 through λ_7 must be blocked from the output and all other wavelengths should pass to the output unimpeded or at least with minimal attenuation.

Figure 9 also shows that, if necessary, the analog input signal may first undergo electronic signal conditioning and sign bit extraction. Generally, signal conditioning may include level shifting and amplitude conditioning such as logarithmic amplifiers. These capabilities (sign bit extraction, signal conditioning, etc.), although typically present in electronic ADC systems, are mentioned here for completeness, and do not imply that the system will not otherwise perform without these components. Additionally, if the return loss of the splitter does not sufficiently suppress optical energy reflected back from the processor filter elements to the source, then an isolator is included in the circuit, as shown in the figure.

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[2] Note that Table 1 quite arbitrarily associates wavelength λ_0 with the binary word {0111}. The cyclical character of the Gray code allows the starting wavelength λ_0 to be associated with any desired binary word (although the number of required filter elements may increase).

Table 1. Four-bit logic table.		
Wavelength Assignment	Binary Count MSB LSB	Gray-Coded Count
$V_0 \rightarrow \lambda_0$	0 0 0 0	0 1 1 1
$V_1 \rightarrow \lambda_1$	0 0 0 1	0 1 1 0
$V_2 \rightarrow \lambda_2$	0 0 1 0	0 1 0 0
$V_3 \rightarrow \lambda_3$	0 0 1 1	0 1 0 1
$V_4 \rightarrow \lambda_4$	0 1 0 0	0 0 0 1
$V_5 \rightarrow \lambda_5$	0 1 0 1	0 0 0 0
$V_6 \rightarrow \lambda_6$	0 1 1 0	0 0 1 0
$V_7 \rightarrow \lambda_7$	0 1 1 1	0 0 1 1
$V_8 \rightarrow \lambda_8$	1 0 0 0	1 0 1 1
$V_9 \rightarrow \lambda_9$	1 0 0 1	1 0 1 0
$V_{10} \rightarrow \lambda_{10}$	1 0 1 0	1 0 0 0
$V_{11} \rightarrow \lambda_{11}$	1 0 1 1	1 0 0 1
$V_{12} \rightarrow \lambda_{12}$	1 1 0 0	1 1 0 1
$V_{13} \rightarrow \lambda_{13}$	1 1 0 1	1 1 0 0
$V_{14} \rightarrow \lambda_{14}$	1 1 1 0	1 1 1 0
$V_{15} \rightarrow \lambda_{15}$	1 1 1 1	1 1 1 1

As with any digital circuit, it is necessary to ensure that each bit arrives at the output port at the same time. That is, the differential path lengths of each bit-leg, from the point of splitting to detection and storage is critical, and the propagation time corresponding to those differential lengths should correspond to a very small fraction of the desired ADC system speed. Otherwise all bit-leg outputs will not be synchronized to the input signal. This delay equalization is easily achieved by adding the proper amount of additional fixed lengths of optical fiber (path trimmers) to each bit leg as shown in the figure. This (fixed) path length adjustment need not be included if accurate path lengths are provided in manufacturing.

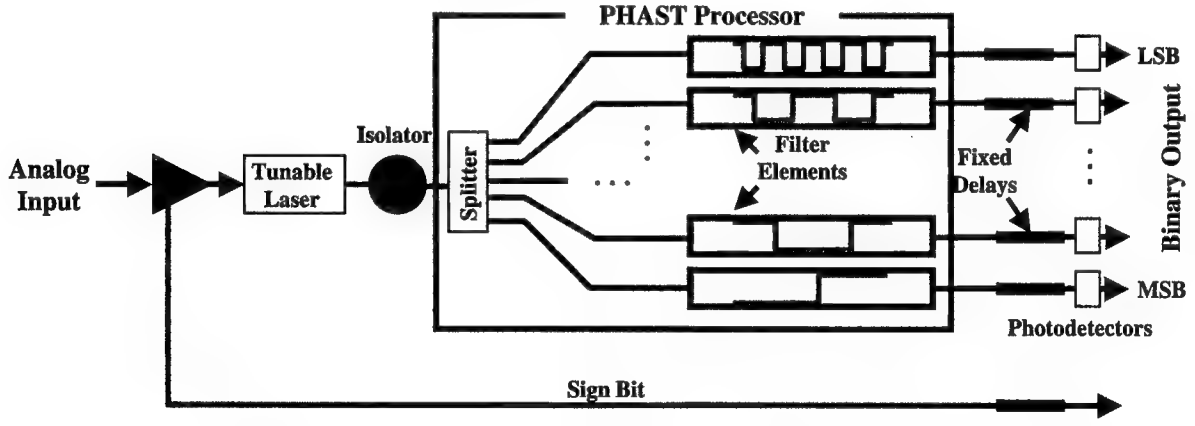


Figure 9. Generic ADC system highlighting processor elements.

3.2 Processor Architecture

The discussion of the processor architecture begins by first considering the use of discrete filters to implement each of the zeros, as required in logic Table 1. Further reduction of

the processor complexity will be realized by recognizing the periodicity in the bit-leg filter transfer function requirements, greatly reducing the required number of discrete filter elements at the expense of greater filter transfer function complexity per bit-leg. A number of approaches exist to realize these filter functions, as described in Section 4.

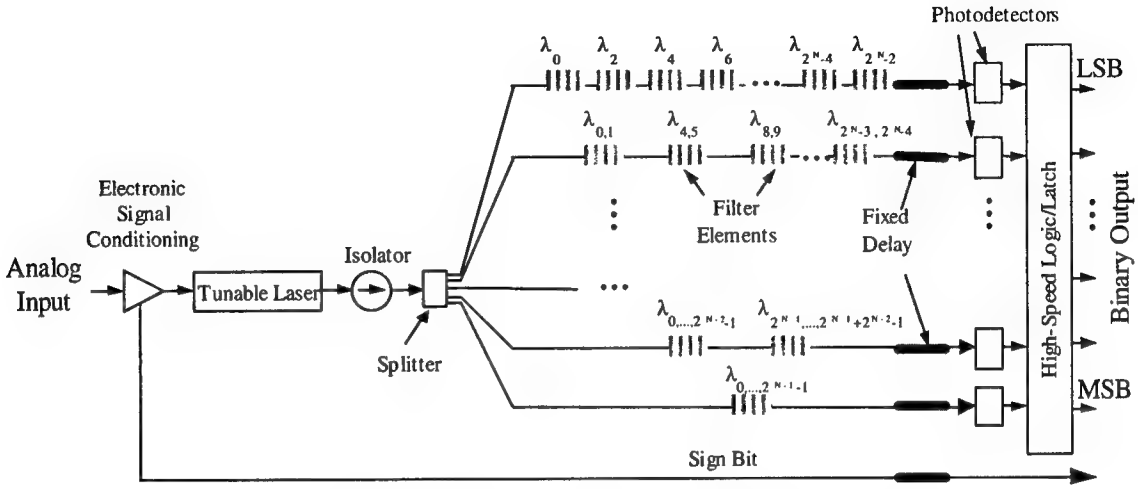


Figure 10. Basic ADC architecture with standard binary count.

3.3 Processor with Discrete Filter Elements

Figure 10 is a standard binary count realization of the processor using discrete filters. With the binary count configuration, we have the option of using one filter element to create a logical zero for each of the required zeros in the logic table. This requires a large number of filters elements, specifically $N2^{N-1}$ elements. Alternatively, a reduction in the number of discrete filter elements can be realized by noting from the logic table that the zeros occur in groups (at least for all bits other than the LSB). This grouping implies the need for broader bandwidth filters, but if fully taken advantage of, results in a factor of N reduction in the number of filter elements required, from $N2^{N-1}$ to 2^{N-1}.

Alternatively, the processor can be configured to count using a Gray code. There are two distinctive features of arranging the binary word in this way. First, the characteristics of the Gray code ensure that wavelength quantization errors affect only a single bit transition at each resolution level. This benefit can most easily be understood by referring back to Table 1 and noting that the transition from a logical zero to a logical one never occurs for two bits simultaneously at any given resolution level. Second, the groupings of the zeros minimize the number of filter elements required; specifically, 2^{N-2} discrete filter elements would be required if a design is used that fully takes advantage of all groupings of logical zeros.

3.4 Processor with "Complex" Filter Elements

Referring back to the logic in Table 1, it is seen that the "1" and "0" patterns of each bit-leg are periodic and, in fact, can be realized by a square-wave transfer function. The exploitation

of this characteristic ideally reduces the required number of filter elements to its minimum, namely N (i.e., one filter element for each bit-leg). This approach closely resembles the system depicted in Figure 2. Further reduction would only be possible if the bit-legs could share a single filter element that could be tapped at the appropriate point along the filter element prior to detection.

A point to be emphasized is that the ADC configurations considered here are not unique, and many other topologies exist, each of which may be determined by different arrangements of the processor filter elements. For example, we have assumed that a *logical zero* is established by the reflection of the *undesired* wavelength *away* from the detector. Another approach would be to reflect a binary one and transmit a binary zero. In addition to using reflection, there are a variety of other methods to effectively achieve a logical zero including absorption (i.e. loss), switching, or non-linear processes. Of course, ideal filters with zero transition widths do not exist in practice. These non-ideal filter issues are considered in the following section.

3.5 Filter Transition Requirements

One of the primary requirements for the PHAST filter design is the width of the transition region, since inappropriate width could result in erroneous binary output. Hence, the focus of this section will be the specification of this transition to minimize the possibility of this error. There are two conceptual approaches that we will consider for implementing the bit-leg filters: an all-passive approach, and an approach that uses a combination of active and passive components.

For the purpose of this discussion, it is assumed that the laser linewidth is sufficiently narrow so that its contribution at the detected output does broaden the transition width significantly. For example, if the tuning range $\Delta\lambda$ is 50 nm, a 12-bit system would imply that the laser linewidth should not exceed $50/2^{12}$=0.024 nm, corresponding to roughly 3 GHz linewidth. This, of course, makes the narrow linewidth assumption valid for most practical lasers. This calculation also indicates a reasonable minimum requirement for the bit-leg filter transition widths, namely $\Delta\lambda / 2^{B}$, where B is the number of bits. Section 4 will present how combinations of passive filter components can be designed to meet these requirements.

Alternatively, as previously mentioned, active components can be used in the bit-leg structures that will greatly relax the passive filter requirements. Specifically, high-speed electronic comparators can be used at the bit-leg detector outputs. In that case, each filter can be as simple as a Mach-Zehnder interferometer designed to provide the required periodicity at any given bit-leg.

4 Complex Filter Descriptions

This section describes the filters and their configurations for the all-passive processor, as discussed in Section 3. Although many technologies have been considered to realize the all-passive PHAST processor filter transfer functions, there are three approaches that can be considered potentially viable from a cost, availability, flexibility, and performance perspective. The three most promising approaches are Thin-Film Filters (TFFs), Fiber Bragg Gratings (FBGs), and Mach-Zehnder (MZ) filters. Based on the aforementioned criteria, the TFF approach would be the most likely candidate for prototype fabrication, as well as realization as a feasible commercial product.

4.1 Filter Configurations

There are a variety of ways of taking the filter elements and efficiently configuring them to minimize the total number of filters needed, while still achieving the transition requirements. Of course, a single broadband filter could be used for each stop band required, but realizing these filters can be challenging and costly. Other techniques involve cascading filters in one form or another. Specially, there are two approaches that are now considered.

The first method involves cascading sharp transition, narrowband filters with staggered center wavelengths to realize a broadband filter. This composite filter provides a sharp transition, namely that provided by one of the narrowband filters. An example of this method is shown in Figure 11, which shows how this idea may be implemented with TFFs. This figure also shows how the composite transfer function is obtained. Of course, this same idea can be used with a variety of other filter technologies.

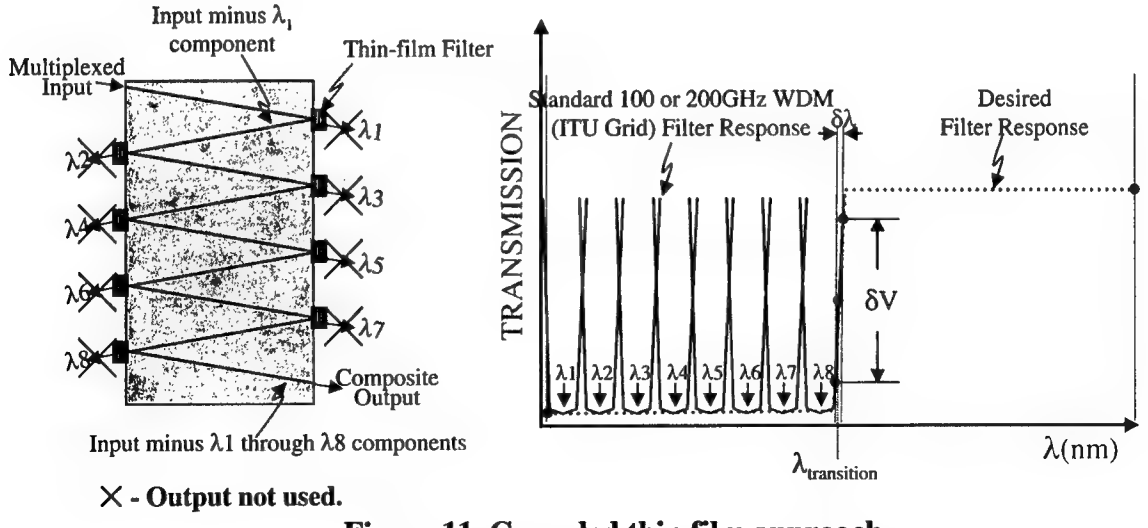


Figure 11. Cascaded thin film approach.

A second method that reduces the required number of filters is the hybrid filter approach. This approach augments a single broadband filter (with unacceptably soft transitions), with one or more narrowband filters on each of the ends of the desired filter wavelength range to sharpen the transitions at the edges. This approach is illustrated in Figure 12.

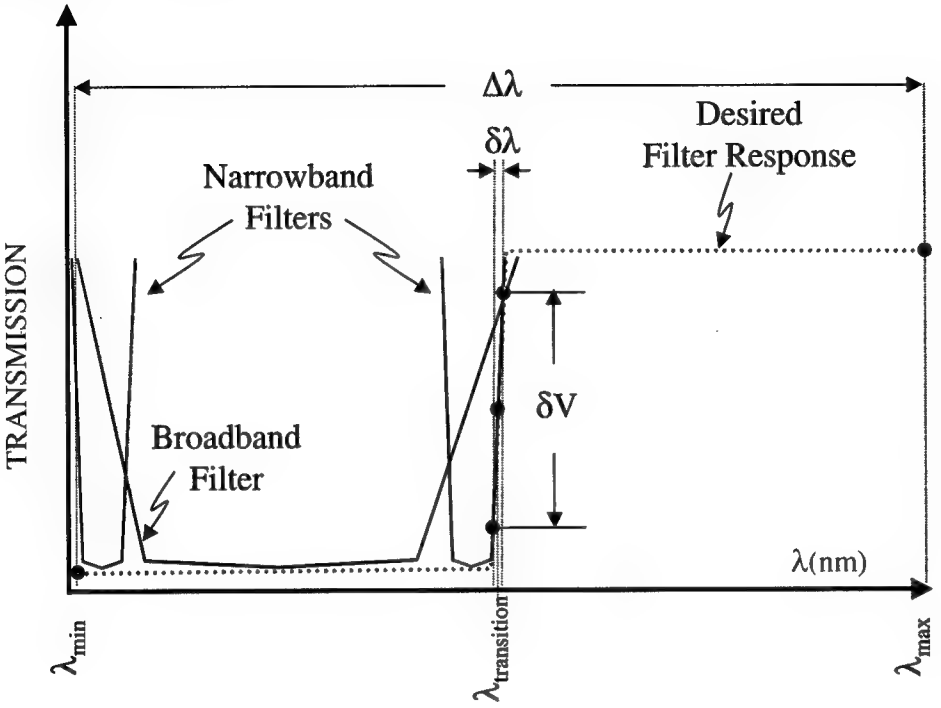


Figure 12. Hybrid filter approach

4.2 Filter Types

The previously discussed filter configurations can be realized through many different filter technologies. As stated, the three most promising are the TFF, FBG, and MZ approaches. Some of the more relevant performance characteristics of these technologies appear in Table 2. The merits of these approaches will be further discussed in the following sections.

4.2.1 Fiber Bragg Grating Filters

The reflection bandwidth and peak reflectivity of FBG filters are readily controlled design parameters. FBG filters with reflection bandwidths as narrow as 0.01 nanometers or as broad as 100 nanometers are available from several manufacturers as commercial off-the-shelf products. Broad reflection bandwidths are obtained by using a chirped rather than periodic index variation. Reflectivity at the Bragg wavelength can be as low as 1% or greater than 99.9%, and off-wavelength transmission is nearly 100%, making FBG filters an extremely efficient and versatile optical design element. The ease of manufacturing and mass production, as well as the emphasis the telecommunications industry has placed on these devices for network applications, will likely result in FBG filters becoming cost effective in the near future.

Table 2. Filter characteristics.

Processor Filters	Wavelength Accuracy (nm)	Channel Spacing (GHz)	Isolation (dB)	Loss (dB)	PDL (dB)	Temp. Coeff. (pm/deg C)
FBG						
ADC Networks						1
Innovative Fibers		62		0.5		0.5
Optical Networks	0.05	100	40	0.2	0	0.7
Thin Film						
Barr Associates						
Kaifa Technology		100/200	25	1.5	0.1	2
DiCon Fiberoptics		100/200	25	1.3	0.1	4
Optical Networks		50	25	7	0.2	0.5
Diffraction Grating based WDM Components						
Photonetics		50/100	4~5	3	0.4	0.5
Fused Fiber						
Arroyo Optics				0.2		0
AWG						
Optical Networks		50	22	9	0.8	10
Interleaver						
ITF Optical Technologies	0.04	100(In)/200 (Out)	20	0.1	0.1	1
Arroyo Optics	0.05	100(In)/200 (Out)	20	0.2	0.1	2

4.2.2 Mach-Zehnder Approaches

Mach-Zehnder filter approaches can be broadly divided into two major types, transversal and cascade. The transversal Mach-Zehnder filter approach includes a splitting element followed by an array of weighted waveguides that have a constant differential path length from array element-to-element, which are then optically summed, leading to a single output. The weights on the waveguides are the Fourier coefficients required to approximate an ideal square wave ($\sin(x)/x$ distribution). As few as ten waveguides can provide sufficient margin required for an 8-bit PHAST ADC. A higher resolution ADC, however, would require many additional weighted waveguides to provide an acceptable transition performance. To realize the required weights in a transversal filter configuration would be extremely involved and such filters do not now exist as commercial products. Therefore, this approach is not considered feasible for the PHAST effort. A cascade configuration of weighted MZ filters suffers from similar limitations.

Another transversal filter approach, one that exists commercially and does not rely on weighted waveguides, is the Arrayed Waveguide Grating (AWG) filter. This device can have greater than 150 waveguides, yielding good isolation (transition margin) between output ports. Although these devices initially look attractive, it is expected that obtaining the bit-leg to bit-leg alignment needed to achieve the PHAST processor requirements would be difficult. This makes the AWG approach unacceptable for the PHAST application.

4.2.3 Thin Film Filter Approach

Multi-layer thin-film filters represent the third filter technology that may be acceptable for the PHAST ADC application. It is possible, using thin film technology, to fabricate very accurate broadband filters with very steep transitions. An example of the wavelength response possible from two commercial broadband TFF devices is shown in Figure 13. It is seen from these plots that these devices can provide very steep transitions. Evaluation of these devices, assuming 30-nm tuning range, indicates that 8-bit filtering is possible. To increase the steepness of the transition of these broadband filters in order to achieve higher resolution filtering would be technologically challenging and, therefore, quite costly.

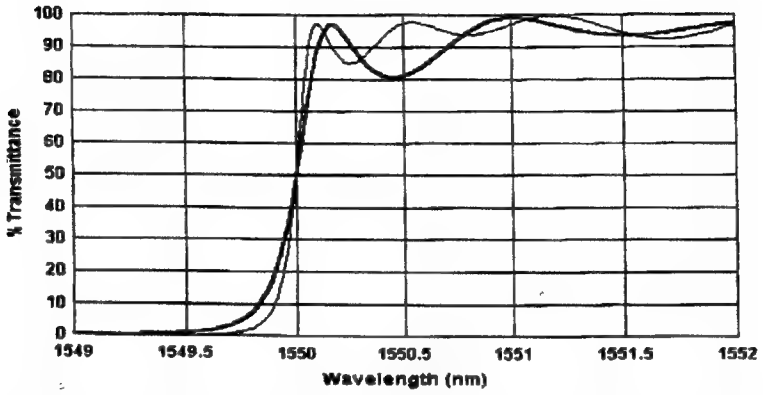


Figure 13. Response curve for two custom Barr thin film filters.

A more practical approach for realizing PHAST optical filters using thin-film filters can be understood by referring back to Figure 11. There, a cascaded array of thin-film filters is shown, each of which is very accurately placed on a single substrate. Each of these filters transmits a specific wavelength and reflects the rest to each successive filter. For the WDM application, it is the through-filter output of each of these filters that is considered the useful (demultiplexed) signal. For the PHAST application, where a square-wave-like filter function is required, this approach must be altered as shown in that figure. In the modified approach, as shown, the thin-film filters transmit the wavelengths corresponding to "zeros" for the desired square-wave filter response, and reflect those corresponding to "ones" to the next successive filter. The desired square-wave-like output then is contained in the composite of all the reflected signals.

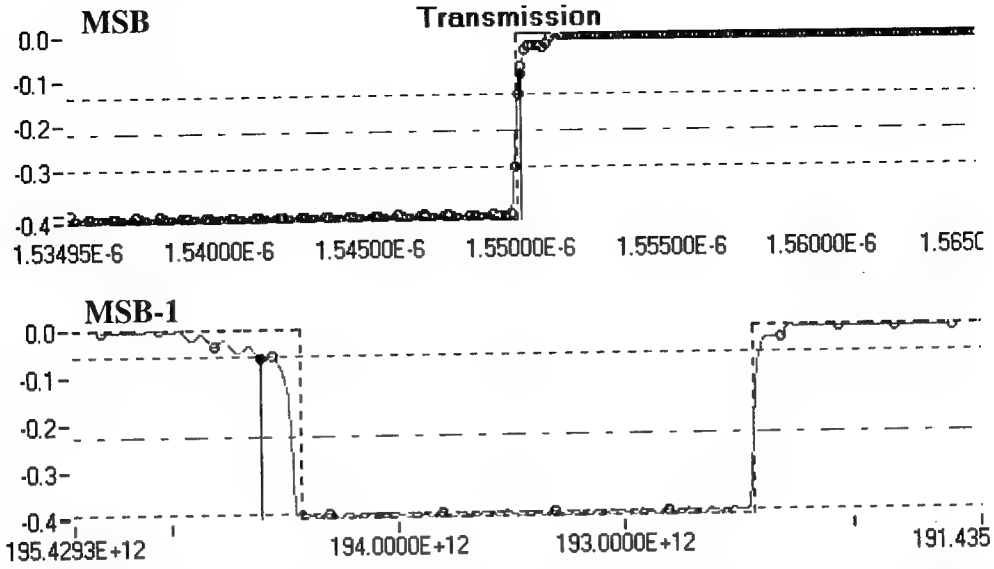


Figure 14. Filter function using DiCon Fiberoptics 200 GHz thin-film WDM add/drop filters.

Another variation on this theme that might be used to realize PHAST system filters involves cascading standard ITU grid 3-port add/drop devices.

Figure 14 shows the resulting filter function realized by cascading several of these commercial off-the-shelf add/drop filters. As stated before, the bit-leg to bit-leg alignment is crucial, and, therefore, custom TFF filters would probably be required to achieve the PHAST processor requirements.

Based on the maturity of the thin-film technology, its flexibility with regard to design, performance characteristics, and the availability of manufacturers, it is readily understood that this technology would offer the best likelihood for successful realization of a basic PHAST processor.

5 Tunable Filter/ Laser Principles of Operation

This section gives an overview of the principles used to design the tunable sources for the ADC application. The sources are of two types: tunable lasers and a tunable filter. Both are different in that the tunable laser tunes over discrete wavelengths, whereas the tunable filter has an envelope that can be tuned in a continuous fashion. The optimal configurations of both the laser and filter are similar in that both contain two Fabry-Perot resonators and an electro-optic phase modulator. The use of an electro-optic phase modulator allows for the possibility of high-speed tuning using a single control voltage. As will be seen, the tunable laser is the tunable filter with gain in a closed loop (ring) configuration.

5.1 Basic Tunable Laser Design

The basic structure for the ring cavity laser is shown in Figure 15, and includes an optical isolator that ensures unidirectional propagation, an optical amplifier that serves as the gain medium, and a directional coupler used to extract a portion of the light from the ring, which establishes the usable laser output. The Fabry-Perot (FP) resonator establishes which wavelengths may resonate, while the actual resonant phase condition is established by the total length, namely

$$2p\pi = n_o \frac{\omega}{c} L_o + n_o \frac{\omega}{c} L_{\text{FP}} + \frac{\omega}{c}(n_o L_{\text{Mod}} + n_o v_{in} \delta L_{\text{EO}}),$$

where ω is the radian frequency, n_0 is the index of refraction (for simplicity, n_0 is assumed equal for all ring components), c is the speed of light, L_{FP} is the length of the Fabry-Perot cavity, L_{Mod} is the length of the phase modulator with no voltage applied, δL_{EO} is the maximum path length change due to the electro-optic effect, L_0 accounts for all excess length, and p is an integer. The tuning is established as follows. The Fabry-Perot only allows resonance to occur at specific (center) frequencies $\omega_i = \omega_{\min} + i\delta\omega$ where $\delta\omega$ is the Free Spectral Range of the FP $\delta\omega = \dfrac{c}{2n_o L_{\text{FP}}}$ and $i = 0, 1, 2, \ldots$. The component lengths are chosen so that at the minimum desired resonant frequency $\omega_{\min}$ and for $v_{\text{in}} = 0$ then

$$2p\pi = n_o \frac{\omega_{\min}}{c} L_o + n_o \frac{\omega_{\min}}{c} L_{\text{FP}} + n_o \frac{\omega_{\min}}{c} L_{\text{Mod}},$$

while for $v_{\text{in}} = 1/2^B$ then

$$2(p+1)\pi = n_o \frac{\omega_{\min} + \delta\omega}{c} L_o + n_o \frac{\omega_{\min} + \delta\omega}{c} L_{\text{FP}} + \frac{\omega_{\min} + \delta\omega}{c}(n_o L_{\text{Mod}} + n_o \frac{1}{2^B} \delta L_{\text{EO}}),$$

where B is the number of bits and where we have assumed that $v_{in_{\max}} = 1$. Specifically, we see that when $v_{\text{in}} = 0$, $\omega_{\min}$ resonates, while $\omega_{\min} + \delta\omega$ is $\pi/2^B$ out of resonance, $\omega_{\min} + 2\delta\omega$ is $2\pi/2^B$ out of resonance, and so forth. The finesse of the Fabry-Perot must be large enough so that these "out of resonance" frequencies are sufficiently attenuated by the overall cavity transfer function.

When the input voltage increases by 2^{-B}, it brings $\omega_{min} + \delta\omega$ into resonance while driving ω_{min} out of resonance by $\pi/2^B$, and so on. Continuing in this way, we see that as v_{in} varies from 0 to its maximum value, the laser cavity linearly tunes from ω_{min} to ω_{max}.

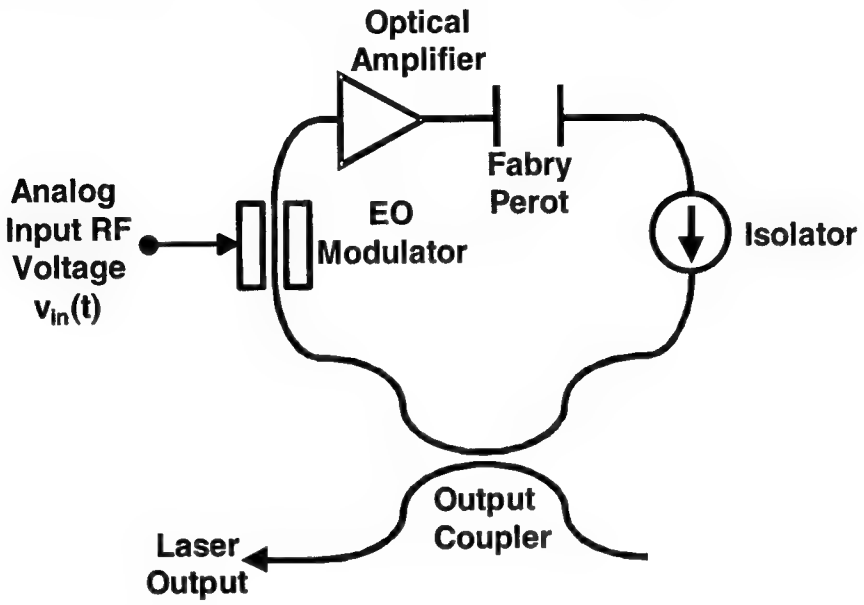


Figure 15. Original configuration before speed enhancements.

5.2 Enhanced Tunable Laser Design

The tunable ring cavity laser described above, though simple in design, suffers from a practical standpoint with regard to mode competition that in turn increases the convergence time of the ring cavity device. This situation is discussed in greater detail in Section 6, where simulated results for this configuration are provided.

A design enhancement that addresses the mode competition concern is shown in Figure 16. It incorporates a second (tunable) FP in the cavity to significantly improve the mode selectivity of the laser. This tunablilty is achieved by placing the phase modulator inside the second Fabry-Perot, as shown. Figure 16 also shows an additional isolator placed between the FPs to prevent the existence of unwanted resonant cavities.

The modes of the two Fabry-Perots are configured such that only a single wavelength can resonate in the circuit for any given voltage and hence mode competition is significantly reduced. This is readily seen with the aid of Figure 17. Specifically, Figure 17A shows the lines established by the fixed Fabry-Perot, while Figure 17B shows those of the tunable Fabry-Perot with zero control voltage applied. It is seen that both cavities have a common resonance at ω_{min}, while the next nearest resonant pair are off-resonance by $\delta\omega$. Tuning the Fabry-Perot by $\delta\omega$ causes both cavities to have $\omega_{min}+ \delta\omega$ as a common resonance, as shown in Figure 17C, with their nearest neighbors out of resonance by at least $\delta\omega$, and so on. We also note that for every 2^B lines of the fixed Fabry-Perot, the tunable Fabry-Perot has $2^B+ 1$ lines, consequently

$$2^B FSR_{\text{Fixed}} = (2^B + 1) FSR_{\text{Tunable}}$$

or

$$\frac{L_{\text{Tunable}}}{L_{\text{Fixed}}} = \frac{2^B + 1}{2^B},$$

where FSR_{Fixed}, L_{fixed} and FSR_{Tunable}, L_{Tunable} are the Free Spectral Ranges and lengths of the fixed and tunable Fabry-Perots, respectively. If 2^B distinct lines are to be resolved, then the Half-Power Bandwidth (*HPBW*) of the tunable Fabry-Perot is

$$HPBW = \frac{FSR_{\text{Tunable}}}{2^B - 1},$$

which then, in turn, specifies the complete enhanced ring cavity system. Section 6 also provides simulation results for this enhanced tunable laser system.

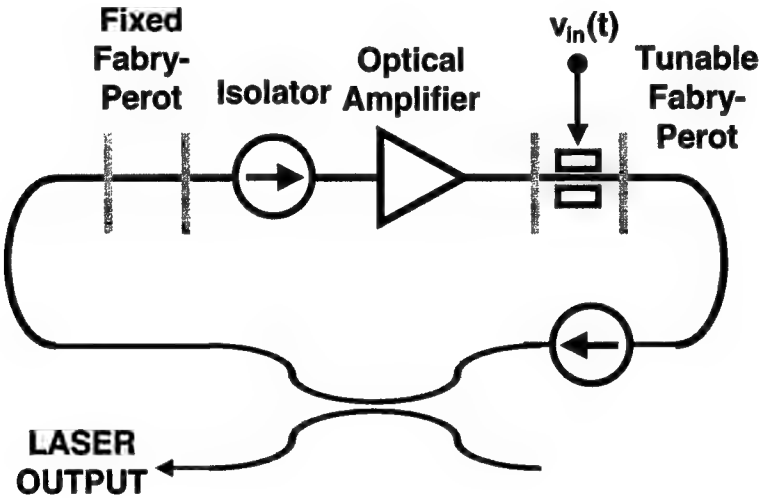


Figure 16. Tunable laser configuration with second Fabry-Perot enhancement.

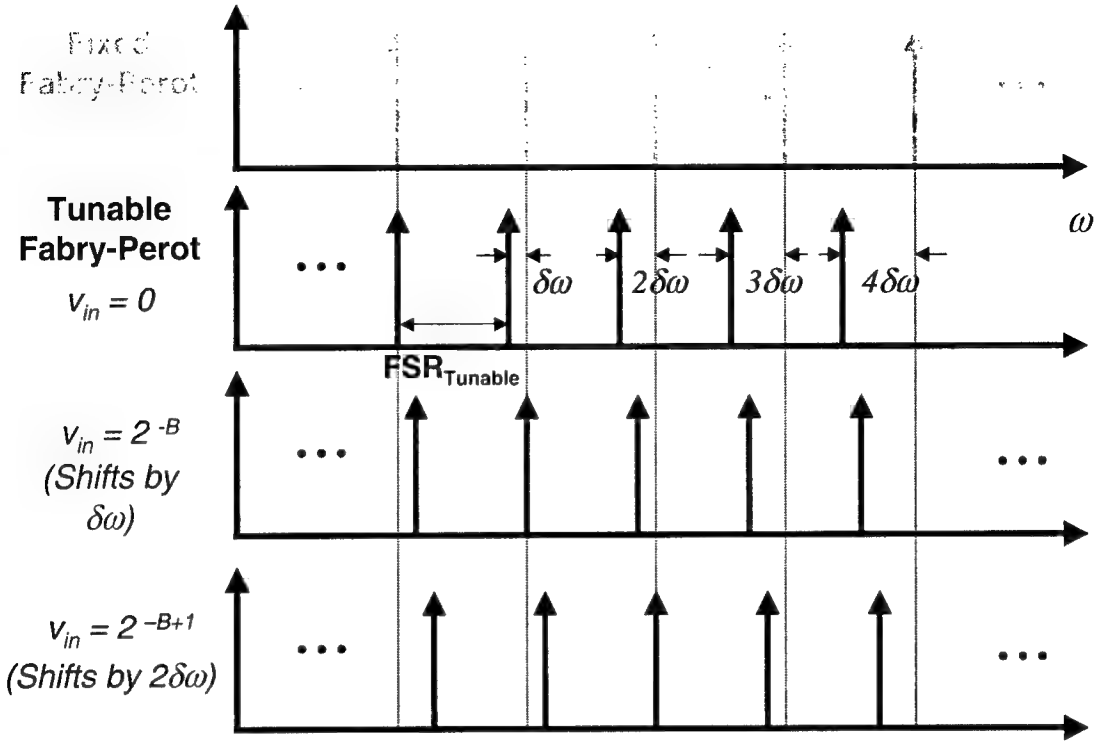


Figure 17. Operation of enhanced ring cavity laser employing a second Fabry-Perot enhancement.

5.3 Tunable Filter Design

The above ring cavity laser approach, which uses two Fabry-Perot resonators, one with an embedded phase modulator, also suggests a means for realizing a passive high-speed tunable filter, as shown in Figure 18 below. The goal of the laser configuration must be to minimize or eliminate mode competition while the tunable filter, operating open loop, can readily support multi-mode operation. Its output would consist of a line spectra established by the fixed Fabry-Perot with a superimposed (tunable) envelope function as a consequence of the overall cavity system transfer function.

The tuning speed of the dual Fabry-Perot filter is determined by the convergence time of the tunable Fabry-Perot. As a general rule, this convergence time is approximately given by the product of the finesse of the tunable Fabry-Perot and its one-way cavity transit time τ. As discussed in Section 7, a Fabry-Perot cavity with an embedded phase modulator will be constructed with a cavity length on the order of 500 micrometers. Using this length, we can estimate the anticipated Fabry-Perot tuning speed as a function of the cavity finesse (bits of resolution). Figure 19 shows the plot of the resolution vs. tuning speed. It is seen that this 500 micron cavity limits the tunable filter finesse to about 16 for 10-Gsps tuning. Therefore, 4 lower bits can be supported with this device, hence, requiring the folding circuit to support the remaining 6 upper bits in order to achieve a 10-bit system resolution at 10 Gsps.

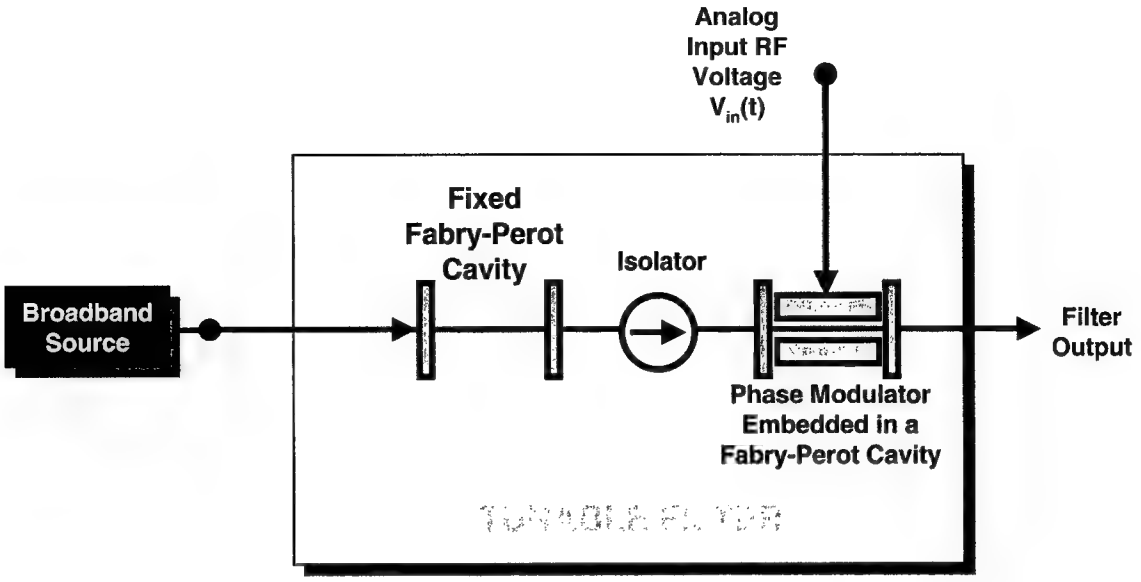


Figure 18. High-speed tunable filter.

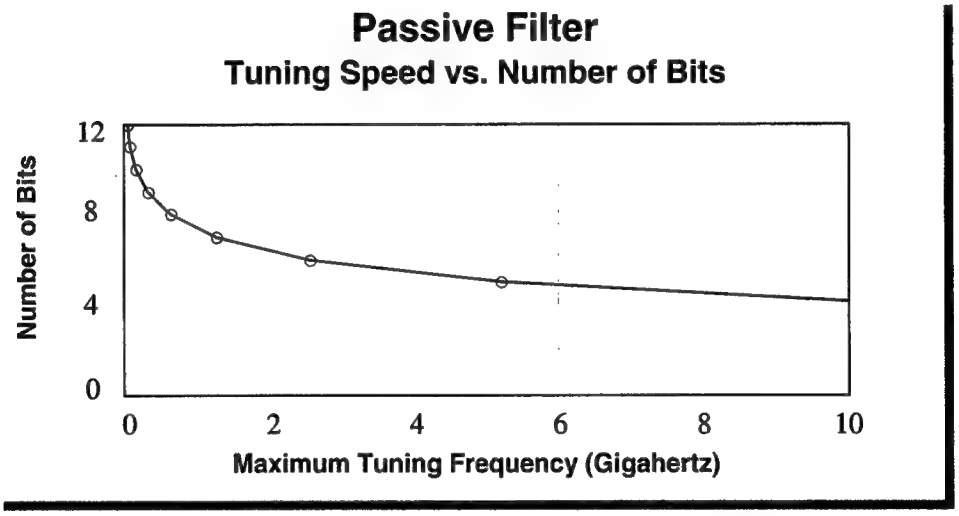


Figure 19. Tuning speed vs. number of bits for passive filter.

6 Tunable Laser Detailed Description and Simulation Results

The basic structure of the tunable laser (TL) is an optical fiber/waveguide ring configuration that contains a phase modulator, a fixed Fabry-Perot (FP) filter/resonator, and a Semiconductor Optical Amplifier (SOA). The basic laser approach is described in some detail in Section 5. Also discussed in that section is the improved tunable laser that, in addition to the components found in the basic TL structure, includes a second FP filter that is tunable over one Free Spectral Range (FSR). The tunability of the second FP is accomplished by incorporating a phase modulator inside the FP cavity.

In the following sections, the simulation approach will be introduced, followed by a discussion of the models, simulation results, and analysis of those results for both the basic and improved TL approaches.

6.1 Simulation Approach

The accurate simulation of the dynamics of the ring lasers under consideration is not trivial, due to the time scales involved for the different devices being modeled. First, to simulate the dynamics of the SOA, which has a gain bandwidth greater than 25 nm, the differential temporal step size of the simulation should be less than 0.32 ps. Second, to simulate the dynamics of the ring, which is on the order of at least 1 cm in the integrated structure, the integration time has to be much greater than 0.1 ns. Third, the dynamics of the FP requires bi-directional simulation. To achieve these capabilities, we simulated the performance of the tunable laser approaches using the Virtual Photonics software package Photonics Transmission Design Suite (PTDS), as well as other user-supplied software modules.

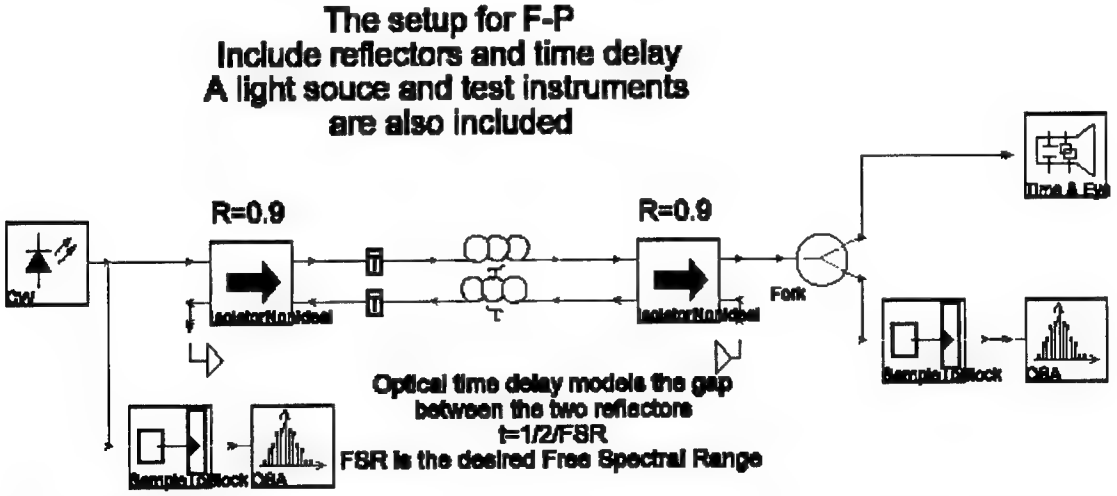
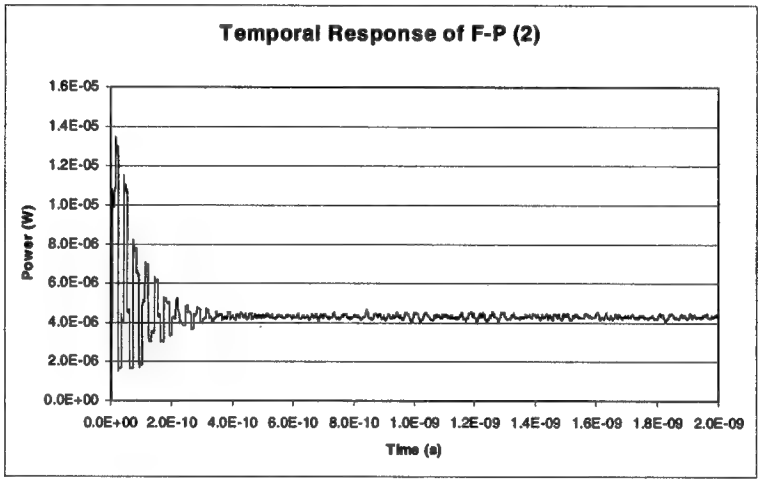


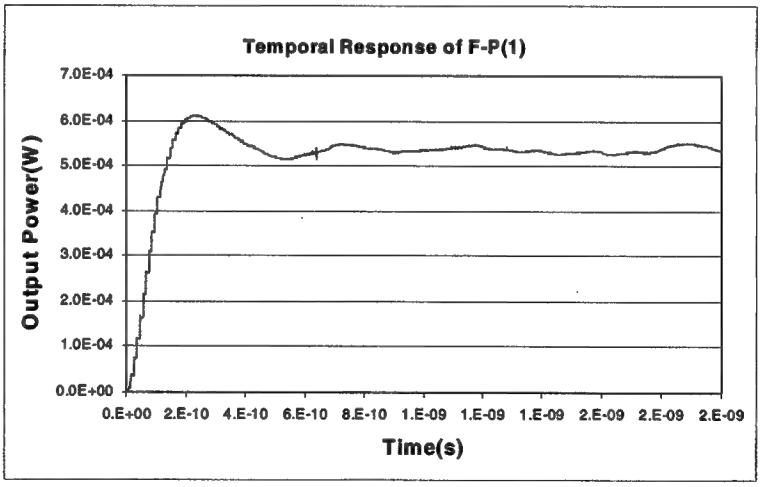
Figure 20. Schematic block diagram of a Fabry-Perot Resonator using non-ideal isolators as partially transmitting mirrors.

To illustrate the capability of PTDS and its appropriateness for the current simulation tasks, simulation of a simple FP resonator was first performed and evaluated. The block diagram of the simple FP is shown in Figure 20. As seen from the figure, non-ideal isolators were used to simulate partially transmitting mirrors.

The transients in the transmission of the FP resonator, on resonance and off resonance, are shown in Figure 21 (a) and (b), respectively. The transient data generated by the PTDS program show good agreement with analytic results.



(a)



(b)

Figure 21. Transient behavior of the transmission of the FP resonator (a) on resonance and (b) off resonance.

6.2 Basic Ring Laser Simulation and Analysis

The major components of the basic ring laser are an SOA, a FP filter, and a phase modulator. The gain bandwidth of the SOA is chosen to be 25 nm, the free spectral range (FSR)

of the FP filter was modeled at 100 GHz, and the FSR of the total ring cavity was set to (5+1/16)*100 GHz. Details are shown in the schematic of Figure 22.

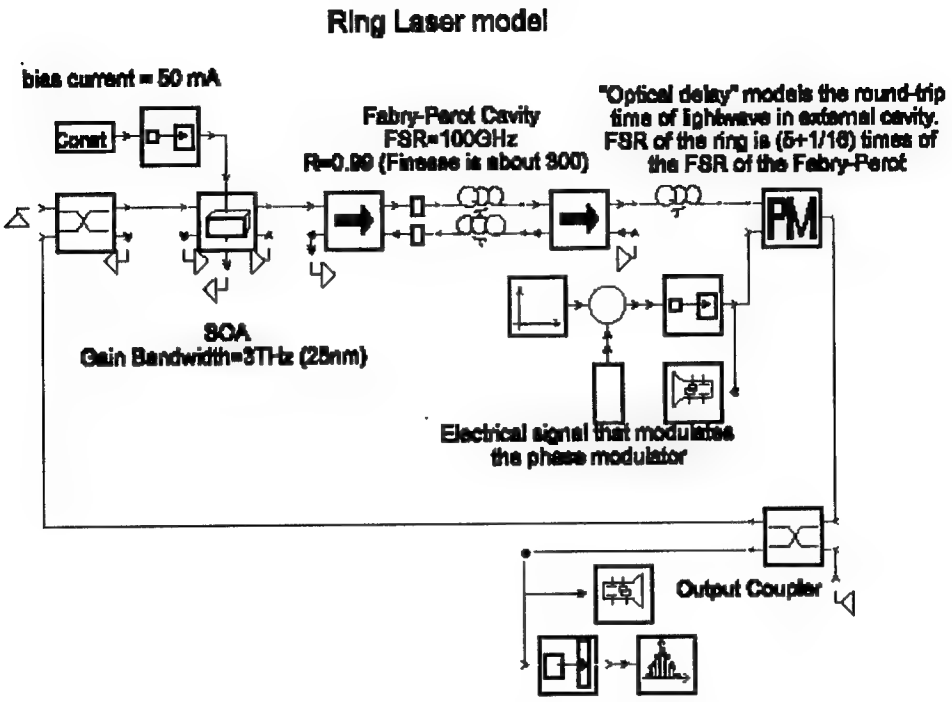


Figure 22. Schematic of the basic ring laser.

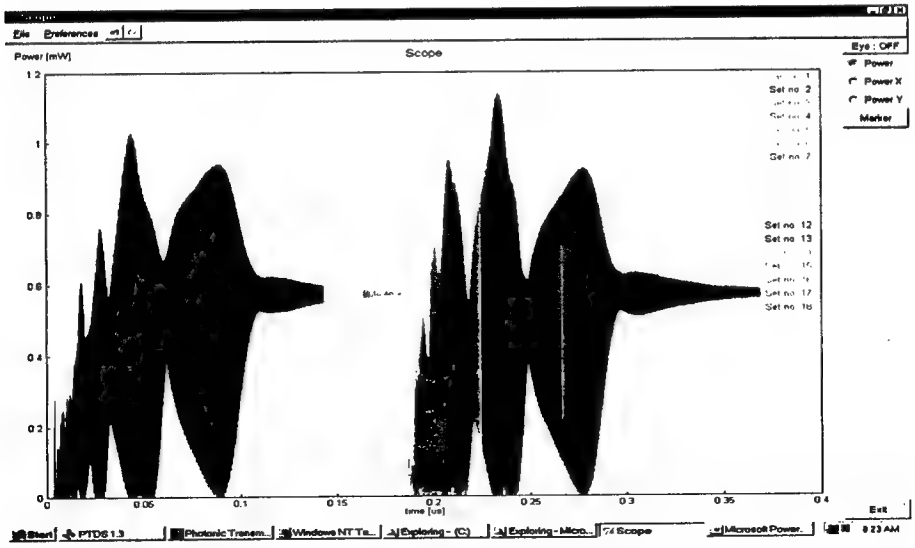


Figure 23. Turn-on and tuning characteristics in the time domain.

The turn-on transients and tuning characteristics in the time domain are shown in Figure 23. DC bias was turned on at time t = 0 and a step function is applied to the phase modulator at time t = 184.32 ns. It can be seen from the figure that the time constants for turn-on and tuning

are on the order of 200 ns, very slow in view of the goal of a 10-GHz ADC. Fortunately, as will be shown, the turn-on transients and tuning characteristics in the spectral domain offer information that will lead to significant improvement of the tuning speed.

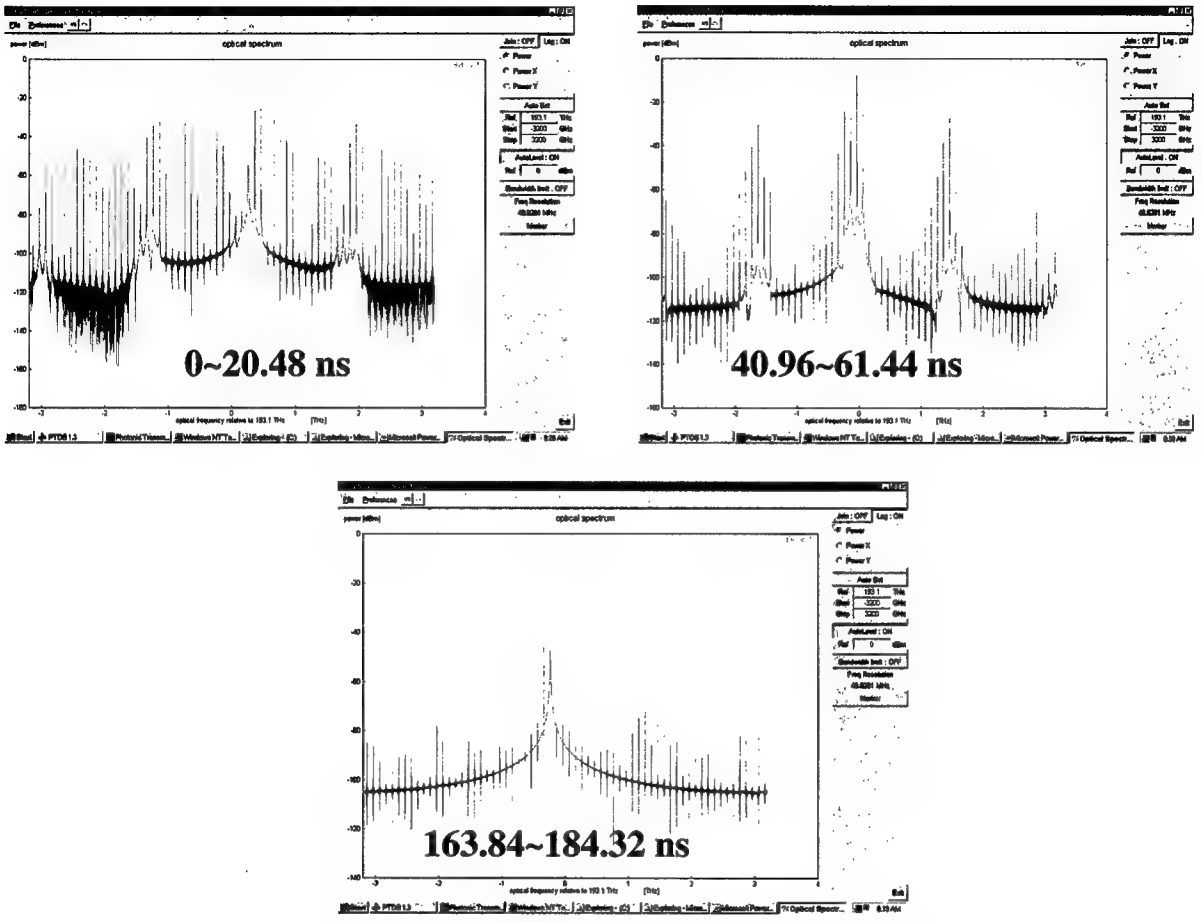


Figure 24. Evolution of the laser spectra during turn-on.

Figure 24 shows the evolution of the laser spectra during turn-on. It is obvious from those plots that the dynamics of the basic TL structure are dominated by mode competition. During the first 20 ns or so, all modes of the ring cavity compete on an equal footing. Between 40 and 60 ns, ring cavity modes within the periodic transmission windows of the FP filter gain competitive advantage. The dominance of one of the FP transmission peaks was established at about t = 100 ns, while complete dominance and amplitude stabilization was seen to take a much longer time, about 180 ns.

Figure 25 shows the evolution of the laser spectra for the basic TL during tuning. It is again obvious that the system dynamics are dominated by mode competition. In fact, the characteristics of mode competition are almost identical to those during turn-on (cold start).

6.3 Improved Ring Laser Simulation and Analysis

Based on our evaluation of the basic TL, we developed an improved tunable ring laser consisting of an SOA and two FP filters. The first FP filter is fixed and a tunable FP filter is added that can be tuned over one FSR via a phase modulator embedded inside the FP cavity. (Recall that the operation of this configuration is discussed in Section 5.) Again, the gain bandwidth of the SOA is chosen to be 25 nm and the free spectral range (FSR) of the FP filter is configured to be 100 GHz. The FSR of the tunable FP is (1+1/16)*100 GHz while that of the total ring cavity is (5+0/16)*100 GHz. Details are shown in the PTDS schematic of Figure 26.

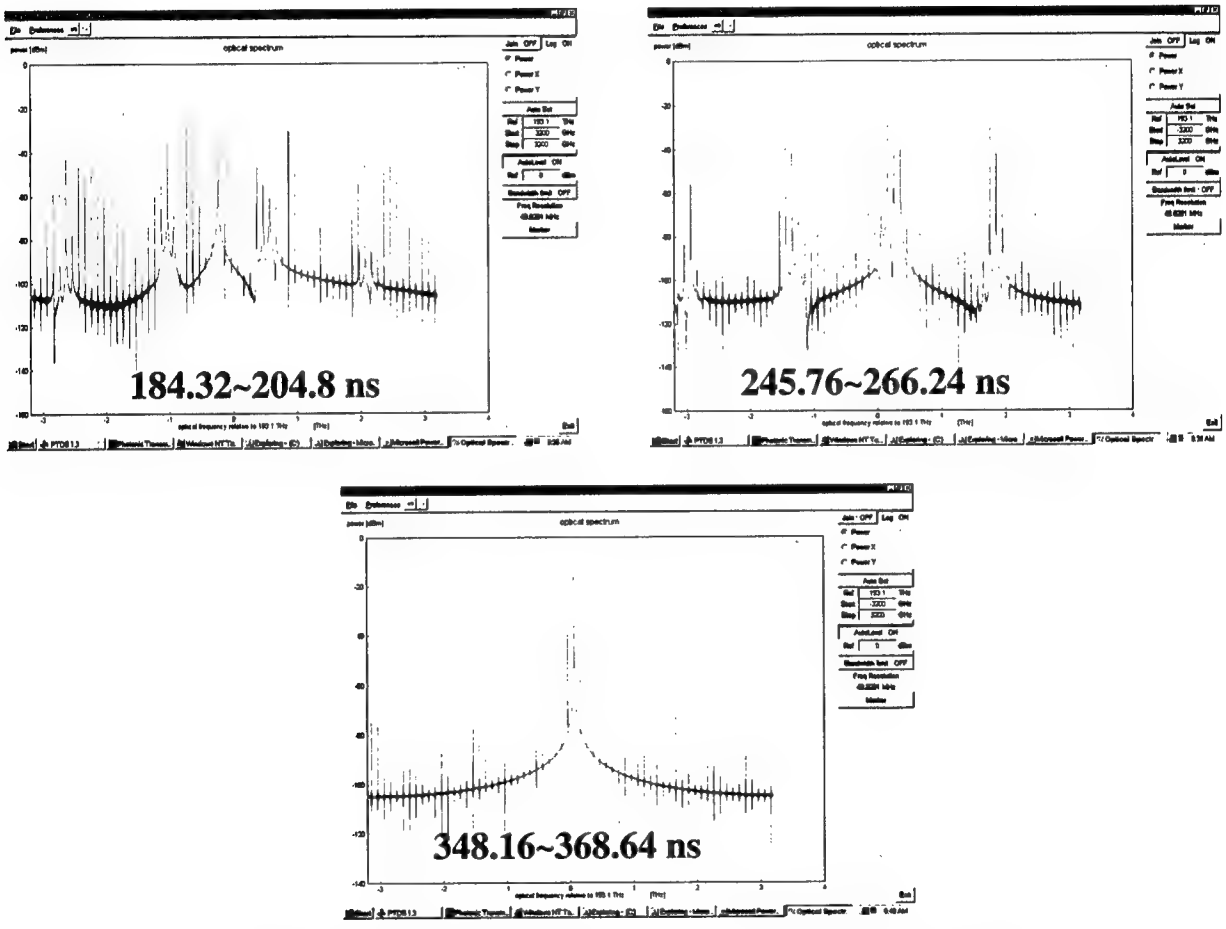


Figure 25. Evolution of the laser spectra during tuning.

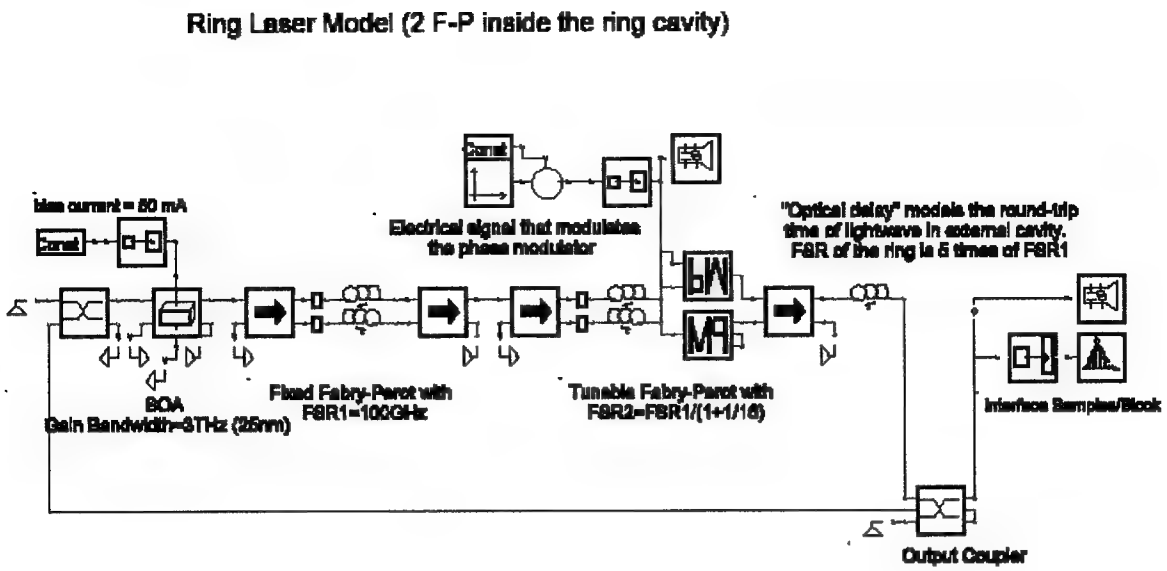


Figure 26. Schematic of the improved ring laser.

The improved TL time domain turn-on transients and tuning characteristics are shown in Figure 27. Direct Current (DC) bias is turned on at time t = 0 and a step function is applied to the phase modulator at time t = 12.8 ns. It is noticed that the time constants for turn-on and tuning are on the order of 8 ns, a factor of 25 reduction in the tuning time when compared to the 200 ns time constant for the basic tunable ring laser.

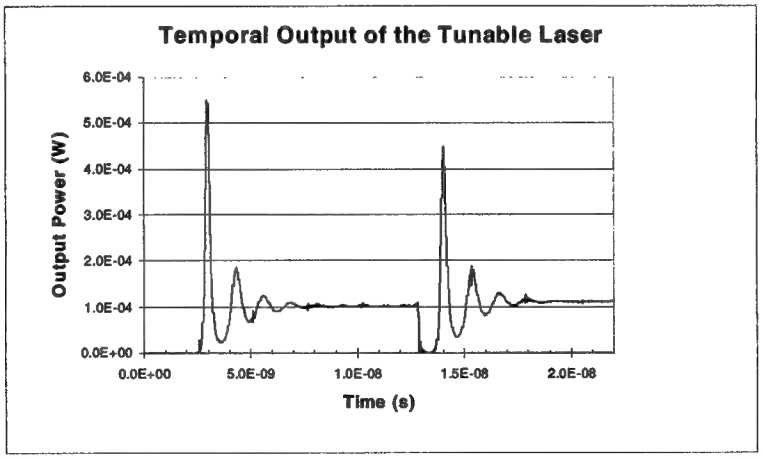


Figure 27. Turn-on and tuning characteristics in the time domain.

The relatively fast turn-on and tuning speeds of the improved TL are related to suppression of mode competition due to the dual FP filters. The suppression is apparent from the turn-on transients and tuning characteristics in the spectral domain, as shown in Figure 28 and Figure 29. From Figure 28, it is observed that mode competition is suppressed. The dominance

of a single mode was established within 2.5 ns. Amplitude stabilization is then dominated by relaxation of the laser, which was accomplished within 8 ns of tuning.

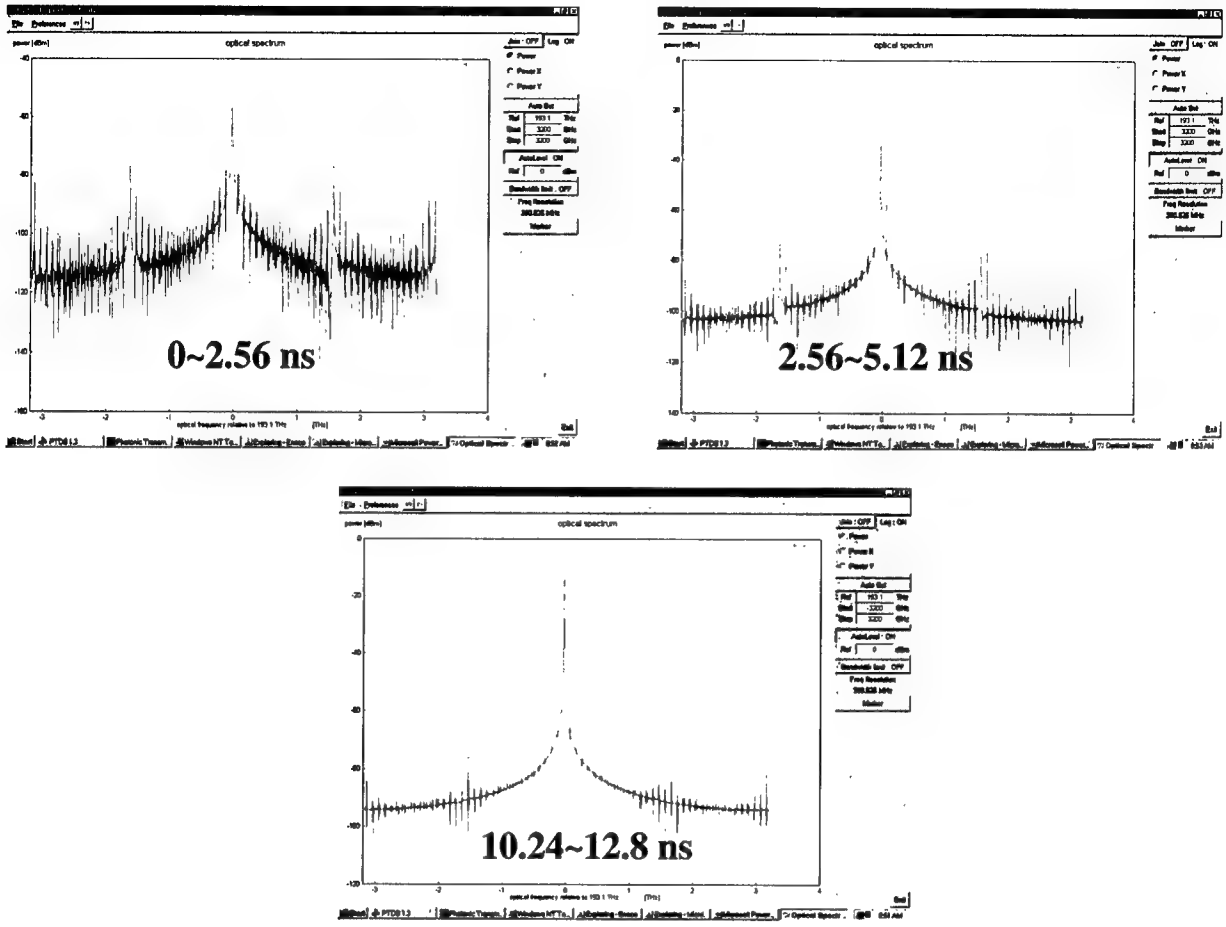


Figure 28. Evolution of the laser spectra during turn-on.

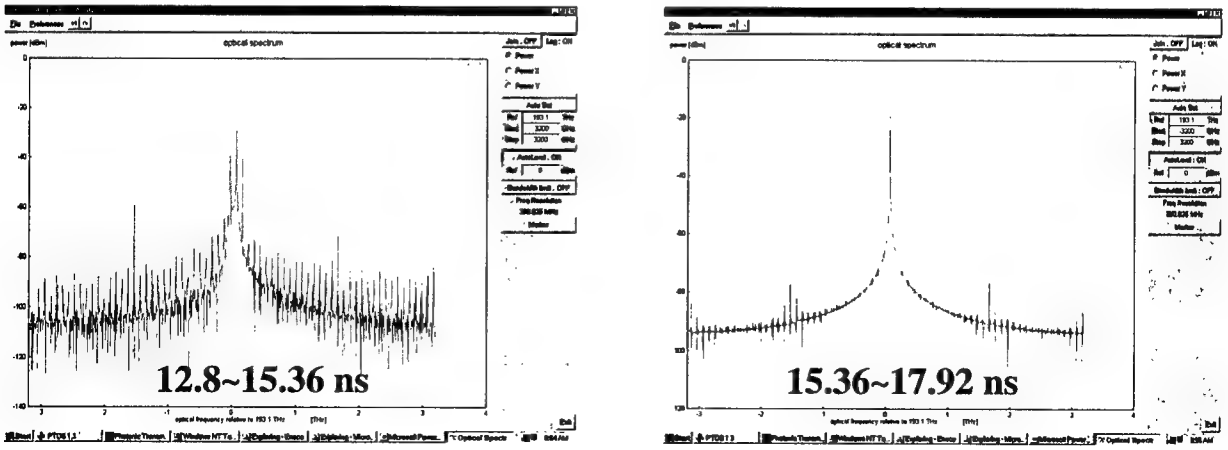


Figure 29. Evolution of the laser spectra during tuning.

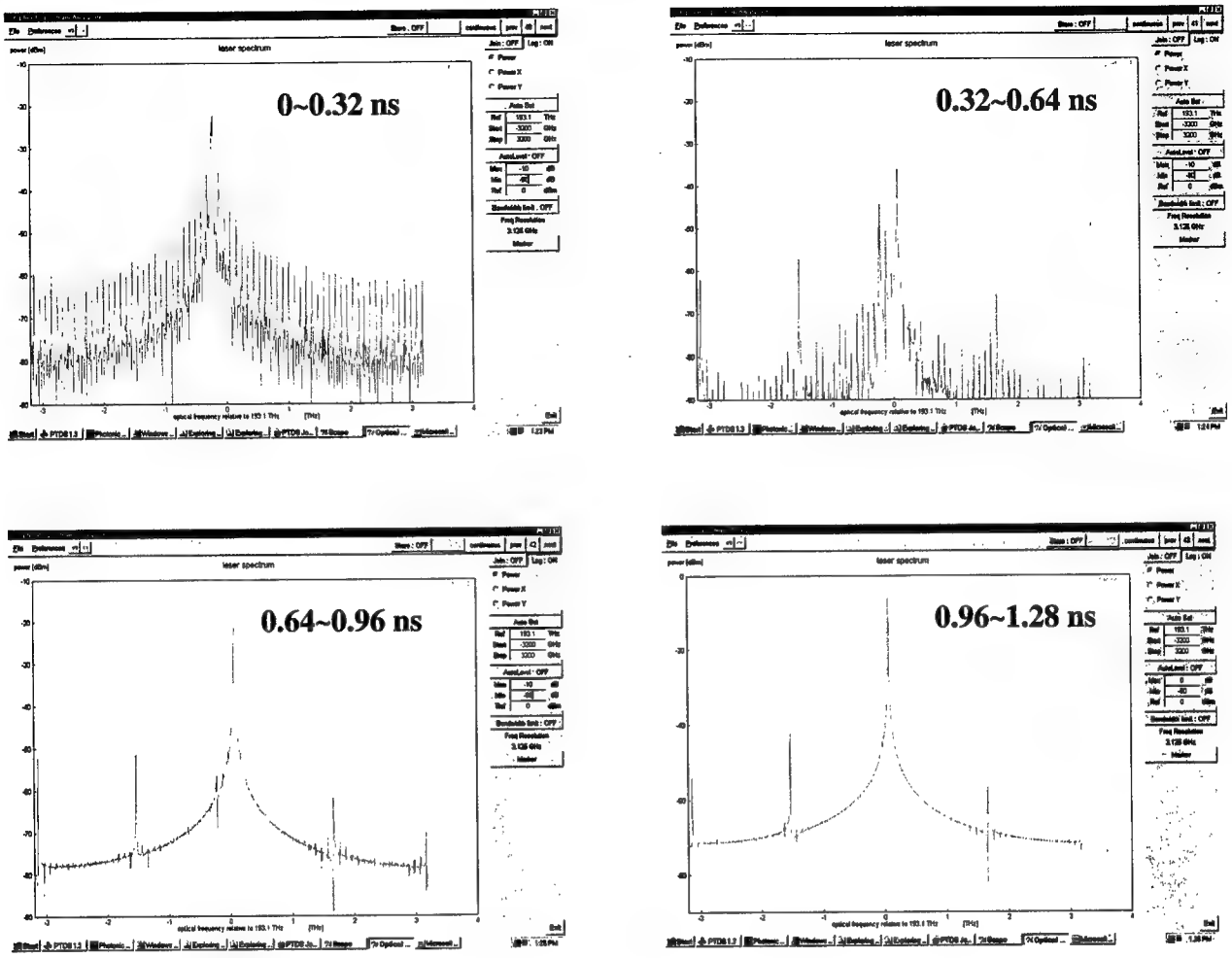


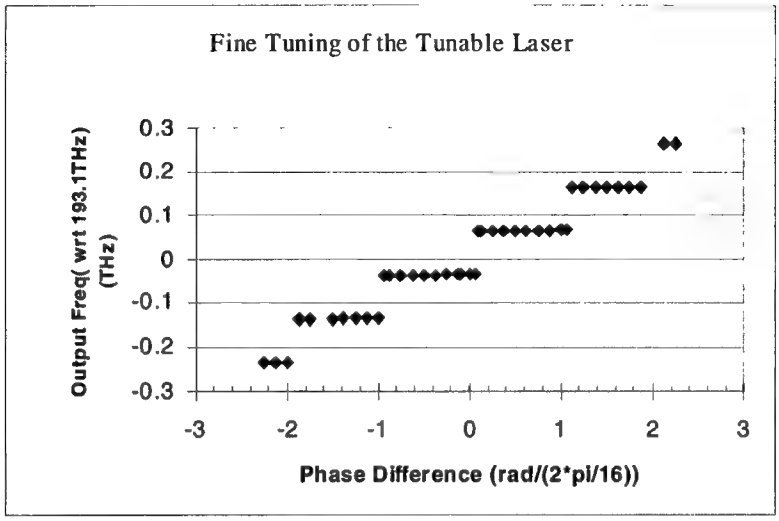
Figure 30. Sub-nanosecond spectral evolution after tuning.

Since the simulation indicates that wavelength stabilization is faster than amplitude stabilization, it is important to further evaluate wavelength-tuning speed. The spectral evolution after tuning is displayed in more detail in Figure 30. As seen from the figure, better than 35 dB of side-mode suppression ratio was established within 0.9 ns.

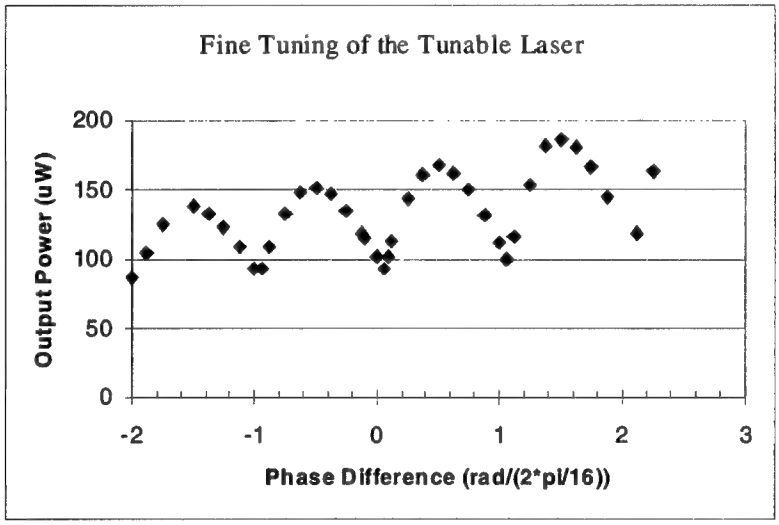
6.4 Output Characteristics of the Improved Ring Laser and Amplitude-Wavelength Coding for the ADC

The steady state wavelength and output power of the improved ring laser as a function of voltage-induced phase difference (change) is shown in Figure 31 (a) and (b), respectively. The figure illustrates two characteristics that are very attractive for ADC applications. First, wavelength tuning is perfectly stepwise, as shown in Figure 31 (a). Within each step, the wavelength stays fixed regardless of the phase change. Second, within each step, output power variation accompanies the phase change, with output power maximized in the middle of each step. As will be discussed, these dependencies lead to an opportunity in achieving a novel

photonic ADC configuration with increased resolution beyond what might be achieved with wavelength tuning alone.



(a)



(b)

Figure 31. Wavelength (a) and output power (b) as functions of voltage-induced phase difference.

The increased resolution capability can be understood by referring to Figure 31 (b). Since within each step of wavelength tuning the output power is a function of the applied voltage, additional and more accurate information is available about the applied voltage and can, therefore, be used to obtain additional bits of ADC resolution. In effect, this amplitude variation is the folded response, as discussed in Section 2.2.1 of this report. One problem that has to be resolved, however, is the ambiguity due to the symmetry of the output power about the main peak within each step. One way to resolve this ambiguity is by using an auxiliary TL in conjunction with the main laser. The auxiliary laser's wavelength tuning is offset by exactly half

the period of the main laser, as illustrated in Figure 32. As a result, when the applied voltage falls within the lower half of the tuning step, the wavelengths of the two lasers are the same. Alternatively, when the applied voltage falls within the upper half of the tuning step, the wavelengths of the two lasers are different. An electronic comparator would then be used to resolve this ambiguity and gives one more bit of ADC resolution.

Because the peak output power is on the order of at least a few milliwatts and received sensitivity is usually less than –23dBm, then taking into account the nonlinear (parabolic) dependence of the output power on the applied voltage, at least four bits can be resolved from this variation. Furthermore, it should be possible to design a laser with $128 = 2^7$ distinct wavelengths (~50 GHz channel spacing and ~50 nm gain bandwidth) resulting in 7 bits of resolution. Again, recall that the dual laser approach provides an additional bit of resolution. Therefore, the combined wavelength-amplitude scheme should provide 11 bits of resolution (since the 7 bits provided by wavelength tuning and the 4 bits provided by the power information are independent) with a 12^{th} bit provided by the dual laser approach. Obviously, reducing the ADC resolution requirement to 10-bit resolution would significantly reduce the technical risk of this approach and appreciably increase the likelihood of success.

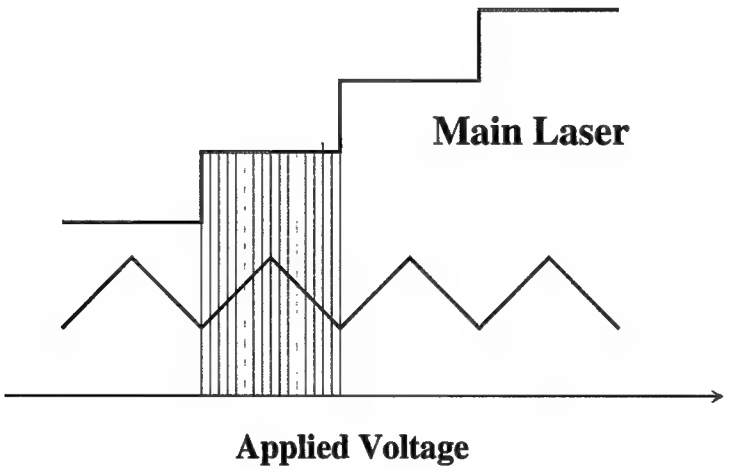


Figure 32. Wavelength tuning and output power characteristics of the auxiliary and main lasers for combined wavelength-amplitude photonic ADC.

6.5 Optimization of Laser Tuning Speed

The remaining issue that must be addressed is the improvement of the tuning speed of the laser. Since the addition of the second FP filter effectively eliminates mode competition, the tuning speed is then related to the response time of the SOA and the ring cavity itself. With otherwise the same component configurations, the temporal dependence of the tuning characteristics due to the length of the ring cavity is shown in Figure 33. It is observed that the tuning speed is only weakly dependent on the ring cavity length as the cavity length is changed from 4 times to 11 times the round-trip optical length of the FP filter. This is expected because the round trip time of the ring cavity is on the order of picoseconds, while the tuning speed is on

the order of nanoseconds. This implies that the tuning speed is primary determined by the dynamics of the SOA.

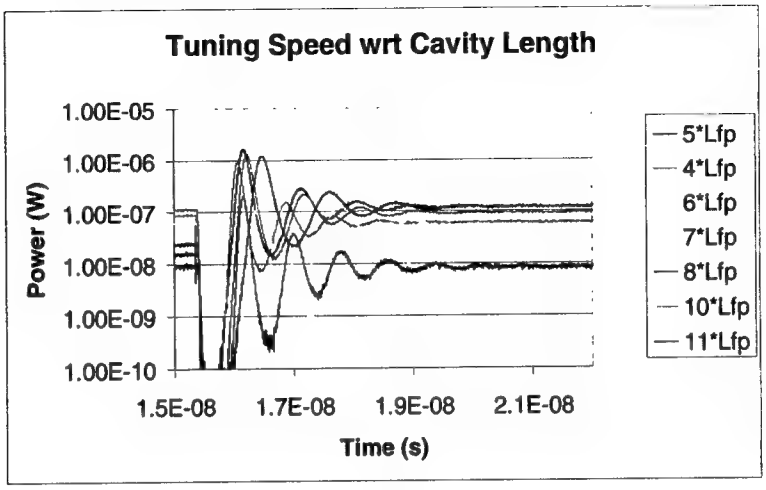


Figure 33. Dependence of the tuning speed as a function of the ring cavity length

The dynamics of the SOA are primarily determined by the stimulated emission lifetime of the SOA, which in turn depends on the bias current and the differential gain. Figure 34 and Figure 35 clearly indicate that the stimulated tuning speed (emission lifetime) increases (decreases) as the bias current and/or the differential gain is increased.

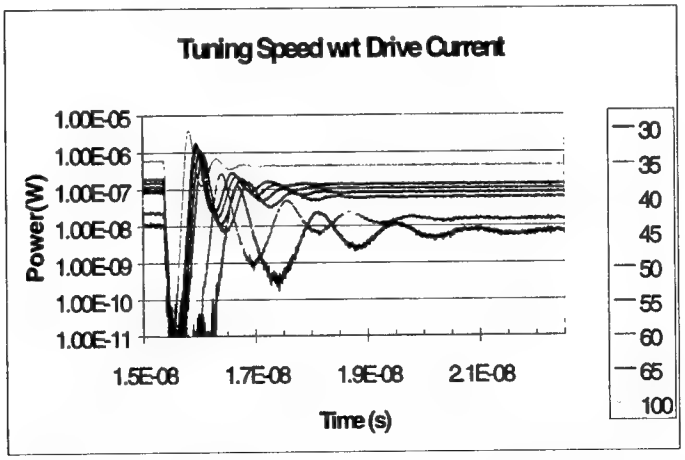


Figure 34. Tuning characteristics as a function of SOA bias current in the range of 30 to 100mA.

The tuning time to achieve both wavelength and amplitude stability can be reduced to 100-200 ps by using high bias current and large differential gain. Figure 36 illustrates a 500 ps tuning time of a laser with the same parameters as in Figure 26, except that the bias current is set to 50 mA and the differential gain is set to 3.0×10^{-20} cm^2.

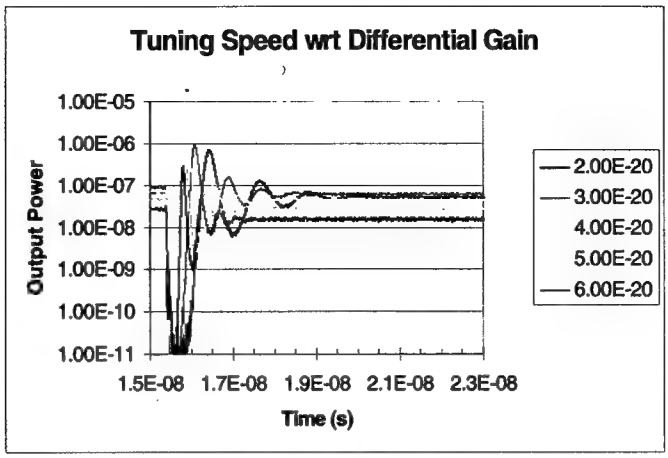


Figure 35. Tuning characteristics as a function of differential gain of the SOA in the range of 30 to 100 mA.

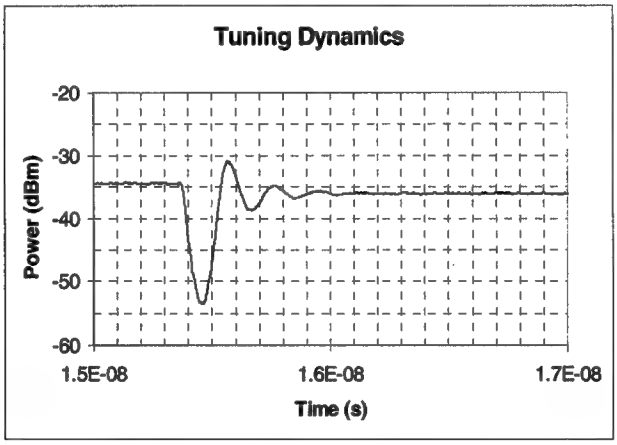


Figure 36. 500 ps tuning of a laser with a bias current of 50 mA and a differential gain of $3.0*10^{-20}$ cm^2.

6.6 Conclusions

- Stable step-wise wavelength-selective tuning has been confirmed.
- For ring cavities with one FP, tuning speed is limited by mode competition. Tuning speed is much less than the FSR of the FP.
- For ring cavities with two FPs, the tuning speed is significantly improved. Based on simulations accomplished thus far, wavelength tuning is established within sub-nanosecond (for 100 GHz FSR) time frames. Amplitude stabilization takes a few nanoseconds. If it is not essential to reach steady-state power, it should be possible to design a laser with 2^7 distinct wavelengths with sub-nanosecond tuning speed. (50 GHz channel spacing, 50 nm gain bandwidth).
- With an auxiliary laser, combined wavelength-amplitude digitization is possible. The dual laser approach provides one additional bit of resolution and, additionally, it should

be possible for the amplitude information to provide another 4 bits of resolution. The combined scheme should readily provide a minimum of 10 bits of resolution at 10 Gsps.

7 Tunable Laser Integrated Device Design

In order to implement the unidirectional ring laser structure in a monolithically integrated device, a triangular waveguide configuration, shown schematically in Figure 37, is adopted. Etched facets at each corner of the waveguiding triangle provide the reflections needed for the laser beam to circulate inside the resonator. Two of the corners of the triangle are cut such that total internal reflections occur and none of the laser energy escapes. The third corner facet (labeled A in the figure) is cut such that the incidence angle is less than the critical angle for total internal reflection and serves as the output coupler. If that facet is perfectly symmetric, then the output coupling from both sides would be equal and the resonator would not be unidirectional. However, in practice, it is impossible to obtain a perfectly symmetric angle and, consequently, there is always an imbalance in the reflectivity of the facet for the optical waves incident on it from the two branches of the triangular resonator. That imbalance is sufficient to cause the laser to oscillate in a unidirectional mode.

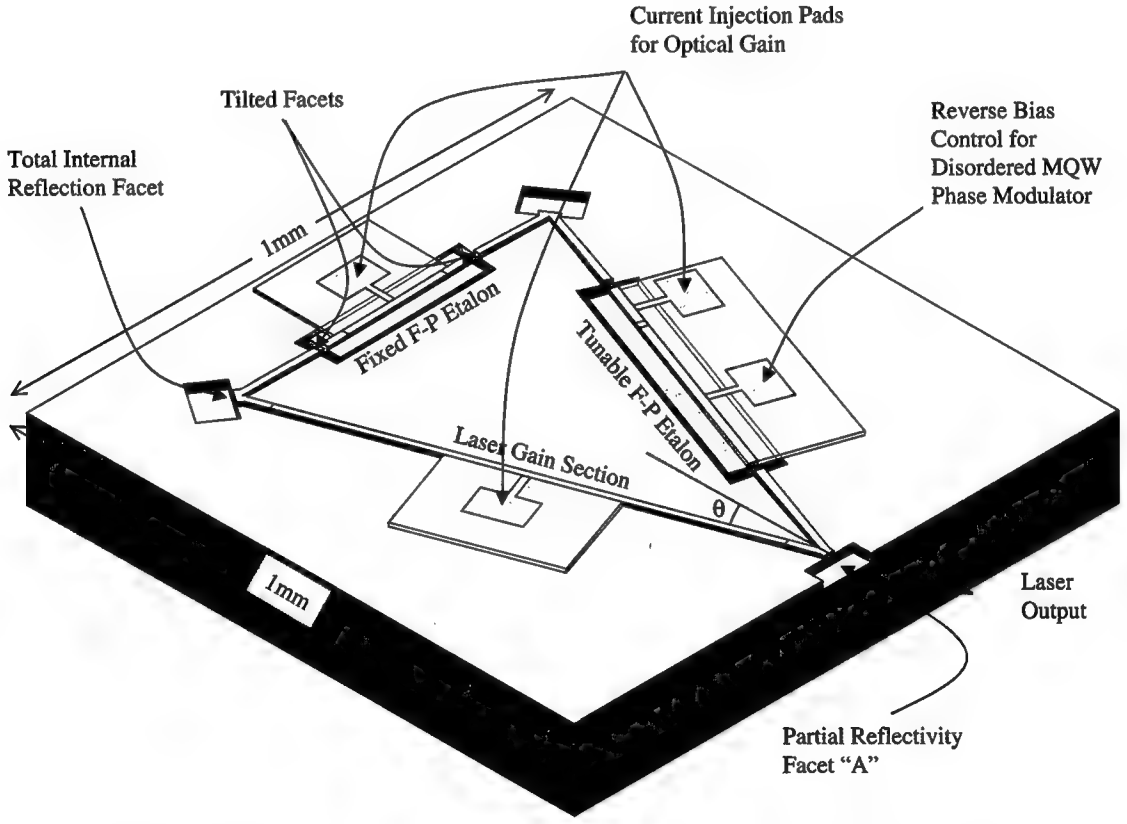


Figure 37. Monolithic wavelength tunable unidirectional ring cavity laser.

The three components of the tunable unidirectional ring laser are (i) the gain medium, (ii) the fixed Fabry-Perot filter, and (iii) the tunable Fabry-Perot filter containing an electro-optic phase modulator. The gain medium is basically the underlying structure, but is confined to one arm of the triangle by current injection in that area alone. The Fabry-Perot filters are achieved by etching mirror facets in the other arms of the triangle. Injecting some current into the Fabry-Perot sections provides optical gain between the etched facets and controls the Q-factor of the

filters. The phase modulator is contained within the tunable Fabry-Perot filter in the third arm of the triangle.

The laser material consists of InGaAs/InP multiple quantum wells (MQW) as the core material bounded by InGaAsP cladding layers. The double heterostructure waveguide configuration is grown lattice-matched on an InP substrate. The structure is designed to provide broadband optical gain peaked at 1.55 μm. In order for the phase modulator section to be integrated monolithically, the optical bandgap of the material in a section of the device needs to be blue shifted to ensure that the material absorption is minimized and electro-optic phase modulation is not accompanied by electro-absorption. The phase modulator section is achieved by selective area disordering of the multiple quantum wells. The material can easily be blue shifted by 100 meV while still retaining characteristics attributable to quantum confinement of electrons. Consequently, the disordered material possesses an enhanced quadratic electro-optic coefficient in addition to the linear electro-optic coefficient. The approximate lengths of the gain and Fabry-Perot filter sections are 1 mm and 500 μm, respectively.

7.1 Component Characteristics and Design Issues

The semiconductor wafer design is shown schematically in Figure 38. It is a typical double-heterostructure laser design containing five InGaAs quantum wells as the active core medium. The gain bandwidth of the active medium is about 40 nm when electrically pumped to very high electron injection levels. With no wavelength-selecting filter present, the resonator would lase at the peak of the gain centered around 1.55 μm wavelength. However, with the use of intra-cavity Fabry-Perot filters, the lasing wavelength is tunable over the whole gain bandwidth. The Fabry-Perot filters are obtained by etching grooves that serve as the reflecting facets. In order to avoid multiple secondary cavities formed by the opposing facets of the grooves, a 4° tilt is incorporated on the facets not forming part of each Fabry-Perot filter. By disordering a section of the MQWs in the second Fabry-Perot filter, the optical bandgap is increased significantly. By placing a metal contact film on that section, a reverse bias is applied to effectively change the refractive index of the core medium and, hence, introduce a variable phase delay and provide tuning capability in the Fabry-Perot. The disordered MQWs are basically distorted quantum wells with graded barriers. Owing to the remnant quantum confinement characteristics, the material possesses both linear and quadratic electro-optic coefficients. The advantage is that a smaller electric field is required to induce a total phase shift of π radians. Typically, for an InGaAs/InP MQW structure, the voltage required for a π-phase shift is on the order of 2 V/mm[1, 2]. In this structure, since the total modulator length is limited to 500 μm, the voltage required to achieve π phase shift is on the order of 1 V. The drawback is that the dependence of the phase shift ($\Delta\phi$) with electric field (E_z) is not linear owing to the quadratic electro-optic components, namely

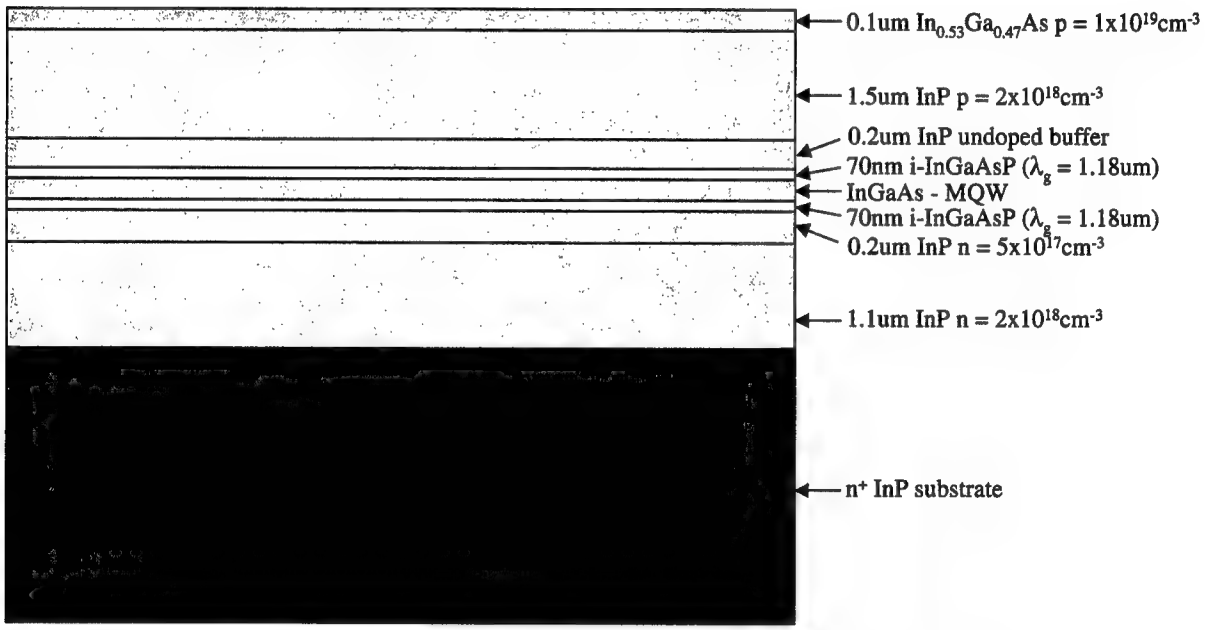
$$\Delta\phi = \frac{\pi l}{\lambda} n^3 \left[r_{41} E_z + (s_{12} - s_{11}) E_z^2 \right],$$

where r_{41} is the linear electro-optic coefficient of InP and s_{11}, s_{12} are the electro-optic coefficients describing the index ellipsoid for the quadratic effect. Consequently, some means of electronic pre-distortion amplifier circuitry would be needed for the ADC to work properly.

The sensitivity of the overall device to temperature fluctuations is primarily dictated by the thermal dependence of the Fabry-Perot cavities. The temperature coefficient of the bandgap is on the order of -5×10^{-4} eV/°C. Although the peak of the gain will shift by 1 nm/°C, the gain spectrum is wide enough that temperature effects are minimized if the temperature is kept constant to within 1°C. The same argument applies to the phase modulator section. On the other hand, the Fabry-Perot cavities are critically dependent on the optical thickness of the etalon. The temperature coefficient of the refractive index of InP-based compounds is on the order of 5×10^{-5}/°C and the thermal coefficient of expansion is 7×10^{-6}/°C. The total phase change is given by,

$$\Delta\phi = \frac{2\pi}{\lambda}\{\Delta n(T).L + n.\Delta L(T)\},$$

where $\Delta n(T)$ is the change in refractive index due to temperature fluctuations and $\Delta L(T)$ is the change in physical length due to thermal expansion/contraction.



MQW is 5 periods 67A $Ga_{0.2}In_{0.8}As_{0.7}P_{0.3}$ / 140A $Ga_{0.54}In_{0.46}As$

Figure 38. Multiple quantum well waveguide layer structure.

Using the above values, we find that the phase change per °C of temperature fluctuation is about 4% of π radians. In order to hold the Fabry-Perot cavities stable to within 1% of π radians, the temperature of the device needs to be maintained constant to within 0.25°C. It is envisaged that the device would be mounted on a thermo-electric Peltier cooler similar to conventional laser diode packaging. The device temperature will be controlled using an electronic temperature controller with a thermocouple or thermistor temperature monitor and feedback, and the whole package will have proper heatsinking.

7.2 Fabrication Issues

At the time we were redirected to stop work on the project, the laser device was at the start of the fabrication phase at the University of Central Florida (UCF) Center for Research and Education in Optics and Lasers (CREOL). The mask design was complete and the wafer had been ordered. The mask set had been drafted using a CAD program and the design was sent to a commercial mask-making facility for a chrome-on-quartz mask to be cut. The mask design included blueprints for the individual devices that would have been fabricated and tested separately. The plan was to fabricate discrete laser chips in order to assess the current density needed to attain optical gain. Discrete electrically pumped Fabry-Perot resonators would have been fabricated in order to determine the highest Q-factor that can be realized as the optical gain is increased to just below lasing threshold. A Fabry-Perot resonator integrated with a phase modulator was also to be fabricated and the tuning characteristics assessed. The semiconductor wafer is a typical double-heterostructure laser design containing five InGaAs quantum wells as the active core medium. The gain bandwidth of the active medium is about 40 nm when electrically pumped to very high electron injection levels. With no wavelength selecting filter present, the resonator would lase at the peak of the gain centered around 1.55 μm wavelength. However, with the use of intra-cavity Fabry-Perot filters, the lasing wavelength is tunable over the whole gain bandwidth.

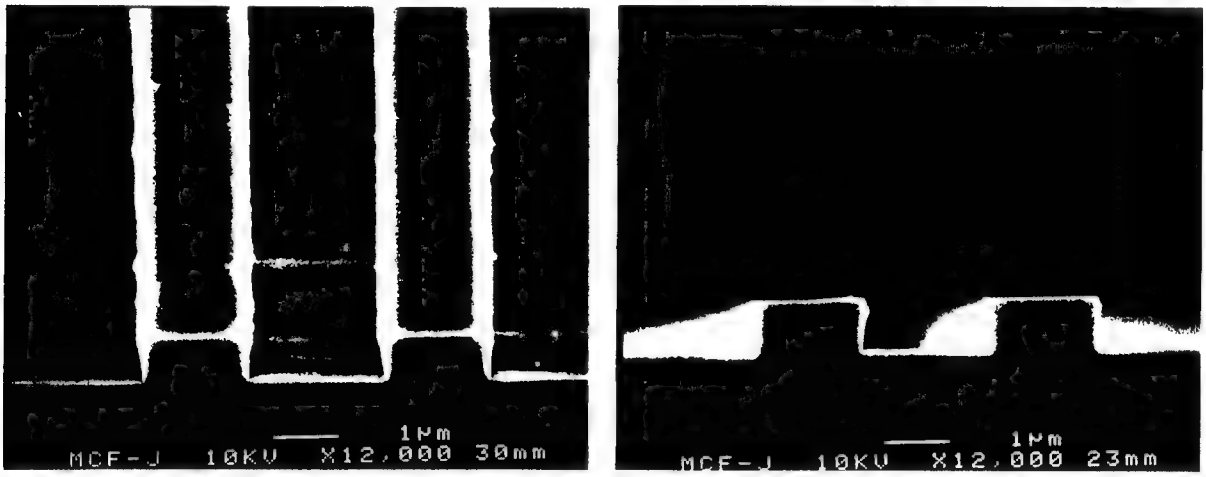


Figure 39. Scanning electron micrograph of features obtained by wet chemical etching of InP.

Fabrication was to use conventional contact mask photolithography and was originally expected to use wet chemical etching. Currently, CREOL is able to use wet chemical etching to achieve almost vertical profiles in InP and InGaAsP compounds, as shown in Figure 39. However, to avoid the possibility that losses at each reflecting facet would be too high, we were prepared to use reactive ion etching in order to define the corner facets. All necessary equipment to permit reactive ion etching was in the process of procurement with PHAST contract funding and matching funds from the Florida High Tech Corridor Council. As a backup plan, we have also considered the purchase of processing time at the Nanofabrication Facility at Cornell University. We planned to employ selective area disordering of the multiple quantum wells to increase the bandgap of the phase modulator section and blue-shift the absorption edge towards the shorter wavelength. Although the same integrated structure can be realized by selective area

etching and epitaxial re-growth, this latter method requires extensive growth capabilities. The main problems appear to be interfacial roughness at the boundaries between the first epitaxial layer and any subsequently grown epi-layer.

Post-growth disordering of MQW layers has been investigated for some time now and that process is now established as a mature technology for the realization of integrated optical devices[3]. MQWs can be selectively disordered in a variety of ways, such as impurity-induced disordering[4], laser induced disordering[5,6], ion-implantation-enhanced interdiffusion[7,8] and vacancy-induced disordering[9,10]. Of these processes, the impurity-free vacancy-induced disordering (IFVD) is ideally suited for electro-optical devices as it does not alter the electrical property of the wafer structures, and waveguides fabricated in such disordered materials do not experience attenuation due to free-carrier absorption.

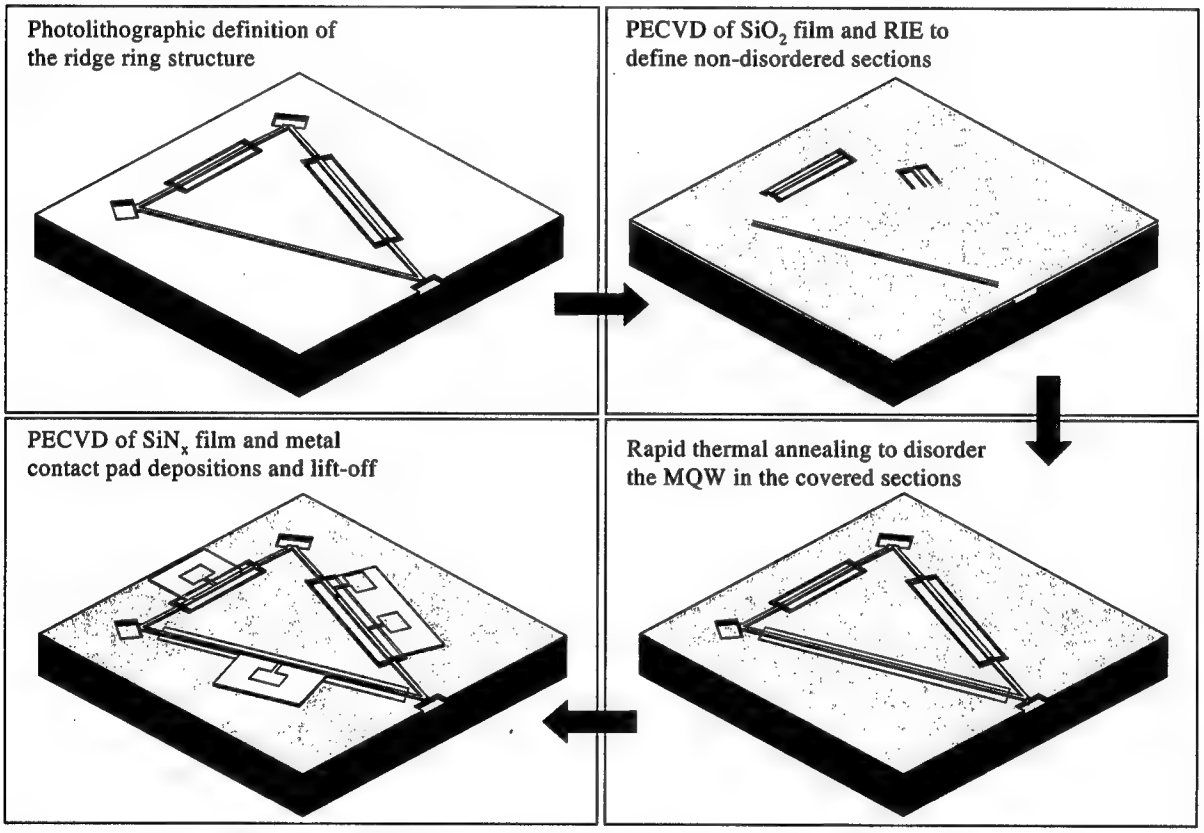


Figure 40. Device processing steps

In particular, we have been working on a simple means of achieving disordering of MQW structures that is also fully compatible with other semiconductor device fabrication techniques. The process is affordable, area-selective, and highly reproducible. We routinely obtain controlled blue shifts of the absorption edge up to 80 meV. These optical bandgap changes have been characterized by measurements of photoluminescence and absorption spectra. In order to achieve controlled localized intermixing between the quantum wells and the barriers, the surface of the sample is coated with a thin film of silicon oxide (SiO_x). The silicon oxide film is deposited using a plasma-enhanced chemical vapor phase deposition (PECVD) process. In regions where no disordering is desired, the SiO_x film is removed by photolithography and

reactive ion etching. The localized compositional disordering is then induced by rapid thermal annealing at elevated temperatures. The magnitude of the blue shift is a function of the annealing time and temperature. The main advantages of this post-growth process are the simplicity of the steps involved and the reproducibility of the results. The interface between the disordered and non-disordered sections is smooth and takes place within a space of 1 μm. The spatial resolution is more than adequate for this particular application.

The electrical contact pads are defined by vacuum evaporation and photolithographic lift-off process. Figure 4 outlines the various fabrication steps. The device is then mounted onto a thermo-electric Peltier cooler and fitted inside a standard 14-pin butterfly package. The device is then ready for testing.

8 Build Approach and Evaluation Schedule

This section describes the build approach and evaluation schedule that would have been used had work on the PHAST project continued. To validate and evaluate the PHAST concepts, the PHAST research team had formulated a build plan and schedule intended to optimize the likelihood of successful implementation of a prototype system by what was then the completion date of this phase of the effort. To minimize the risk in the effort, the original PHAST proposal called for several build phases. Phase I of the effort includes a proof-of-concept (breadboard) build, followed by a prototype system build. The proof-of-concept build phase includes assembly and evaluation of the tunable laser, tunable filter, and folding circuit concepts. The final prototype system, then anticipated to be delivered to the government at the end of Phase I in April 2001, would have provided 8-bit, 10-Gsps analog-to-digital capability using the concepts described herein. Additionally, a Phase II effort was proposed wherein the PHAST research team would develop a fully functional 10-bit, 10-Gsps brassboard system. In the remainder of this section, an overview of the build approach for the Phase I effort will be presented as well as a schedule for its implementation.

8.1 Breadboard Build

The intent of the breadboard build phase is the implementation and verification of the performance of the key components of the PHAST system. The subsystems would have been fabricated on optical benches at the University of Florida, typically using commercial off-the-shelf bulk optical components with the exception of the tunable Fabry-Perot source, fabricated by UCF/CREOL. The performance verification was to be accomplished using the optical and RF instrumentation available at the respective facilities of the team members. The measured performance would have been evaluated by comparison of the results with models that have been developed earlier in the effort by the PHAST team.

8.1.1 Proof-of-Concept for the Tunable Laser

The tunable laser breadboard has been assembled and evaluated. The schematic of the breadboard tunable laser is illustrated in Figure 41 and is similar to the single FP system discussed in Section 5. The single FP system was chosen over a dual FP system breadboard, since our primary goal was to prove the concept of operation of the tunable laser and not necessarily to validate convergence speed. Convergence speed has been evaluated via simulations, as shown and discussed in Section 6, but actual speed measurements on a working laser would have to wait until the much smaller integrated laser could be fabricated.

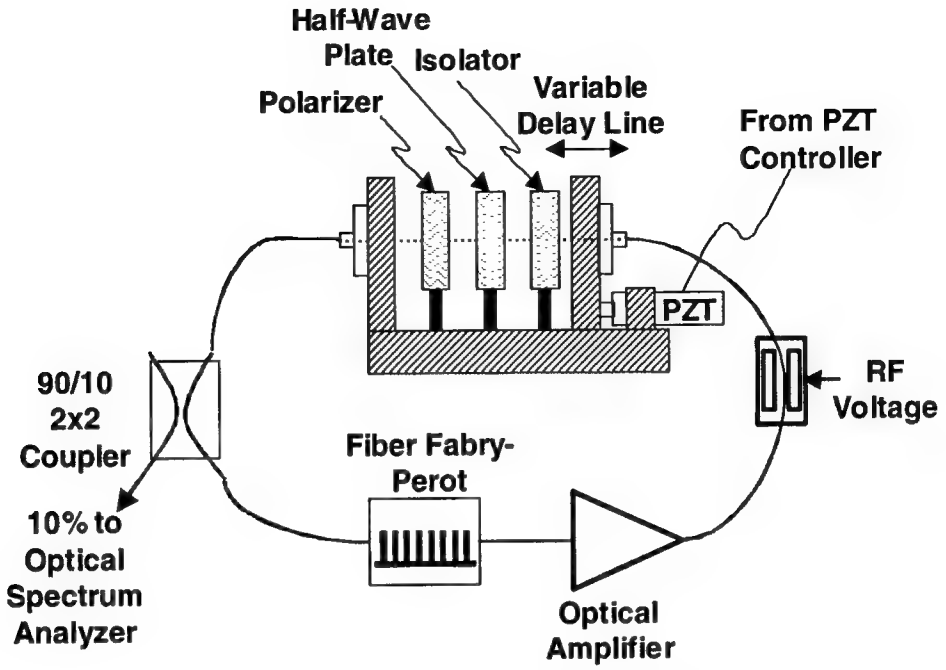


Figure 41. Breadboard tunable laser schematic.

The principle components of the tunable laser experiment included a variable delay line to adjust the fiber ring length. It also gave us the ability to drop in components such as a polarizer, half-wave plate, and isolator. The variable delay line provided course adjustment manually via a high-resolution micrometer or remotely via a stepper motor, and fine resolution via a piezo-electric transducer. The other components included a pigtailed semiconductor optical amplifier, phase modulator, fiber Fabry-Perot, and a 90/10 splitter.

The tunable laser breadboard is shown assembled in the photograph in Figure 42. The breadboarded system demonstrated the ability to tune linearly over a 16-nm tuning range. Some of the laser lines showing the tuning capability of the breadboard system are also presented in Figure 42.

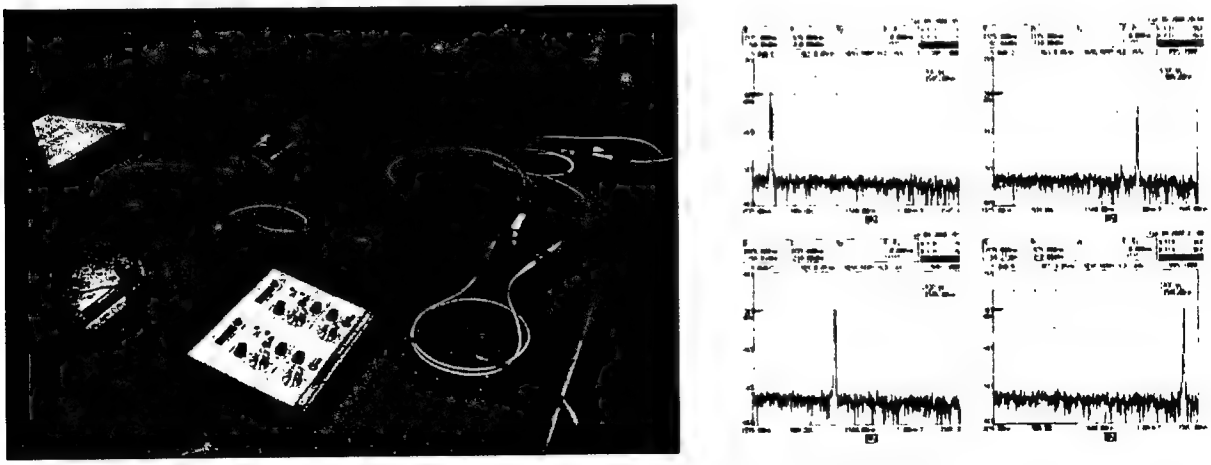


Figure 42. Breadboard tunable laser experiment.

8.1.2 Proof-of-Concept for the Folding Circuit

To prove the concept for the folding circuit, a breadboard system was assembled and tested at the University of Florida (UF) photonics facilities. The folding circuit (including linearization) is similar to the approach shown in Figure 6 and is shown in more detail in Figure 43. The system was composed of two discrete MZ interferometers: one for the folding capability, and the other to provide the proof-of-concept implementation for a first-order linearization circuit. This breadboard system was found to be unsuitable for testing at the desired 8-bit level, due to instabilities and drift in the tabletop components. This drift was primarily caused by birefringence effects in the fiber as well as temperature. Since the folding circuit is interferometric in nature, these instabilities must be eliminated before any meaningful measurements can be taken. It is expected that by integrating the folding circuit architecture in the form of a photonic integrated circuit, these instabilities could be essentially eliminated. At the time we were redirected to stop work on the project, a more compact integrated design was being considered for fabrication and testing.

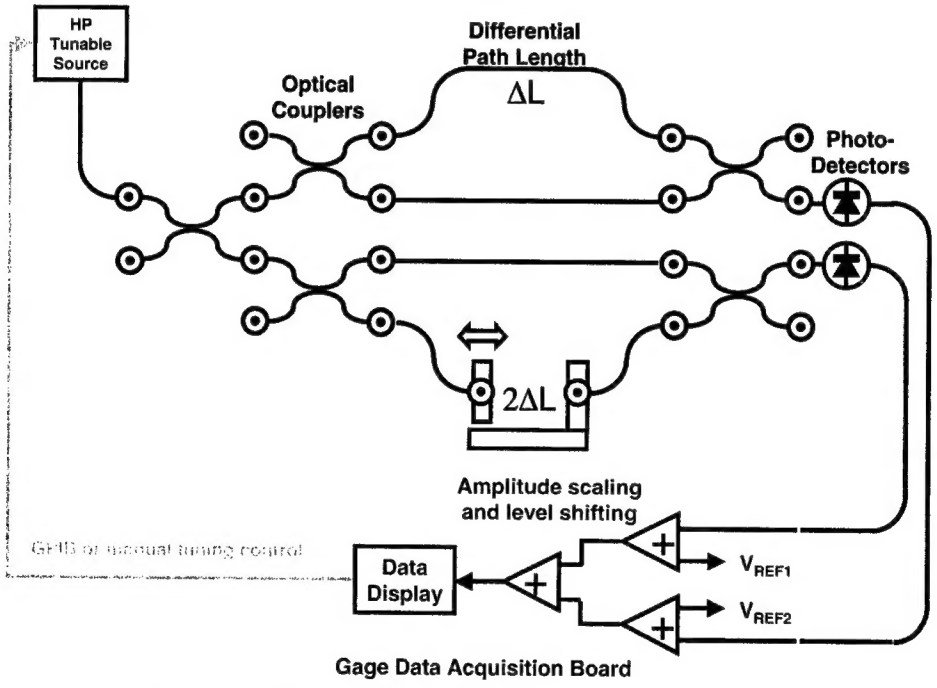


Figure 43. Operation of the linearization circuit.

8.1.3 Proof-of-Concept for the PHAST ADC

The proof-of-concept system described in Section 8.1.2, once assembled and tested, was to have been transported to the test facilities at ENSCO for configuration to a high-speed Tektronix oscilloscope. The oscilloscope can be used to perform real-time sampling out to 8 bits per channel at a 3 GHz rate. Using two of the four available channels on the oscilloscope will result in verification of the performance of the PHAST concept at an effective 10-bit resolution

and 3-GHz rate. The successful completion of this proof-of-concept phase was scheduled to be subsequent to the fabrication, assembly, and testing of the tunable laser.

8.2 Prototype System Build

The proof-of-concept system, described in Section 8.1.2 above, relied on the use of discrete optics (i.e., variable delay lines, optical fiber, and various other bulk optical components) to achieve the stated goal of that section. The prototype system build discussed here would use custom integrated optical components to implement the folding circuit, including any levels of linearization used. The Mach-Zehnder devices were planned to be fabricated at UCF/CREOL. In addition to evaluating LiNbO3 devices, InP and GaAs materials were considered for fabricating these devices.

8.3 Schedule for PHAST Phase I Build

The build and evaluation schedule that would have been used for the PHAST Phase I effort is shown in Figure 44. This is the most recent schedule, as provided to DARPA and AFRL representatives at the DARPA/MTO 2000 Optoelectronics Review in Cincinnati, OH, on 18 October 2000. The schedule details the structure for the execution of the design, fabrication, integration, and testing portions of the proof-of-concept and prototype development phases.

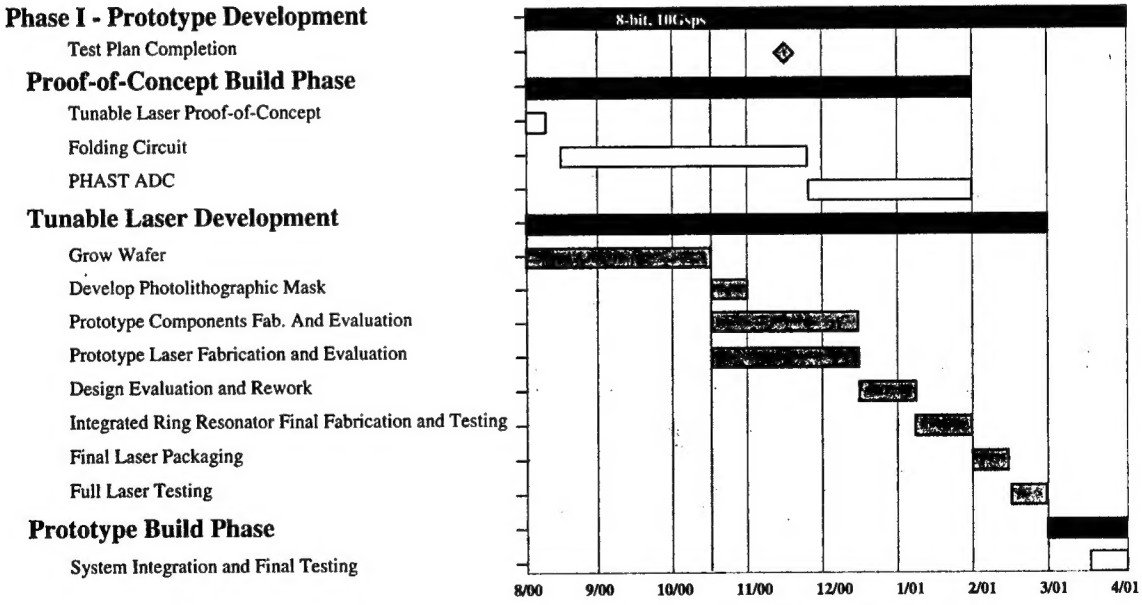


Figure 44. Build and evaluation schedule for Phase I PHAST.

9 Conclusions

The Photonic High-speed Analog-to-digital System Technology (PHAST) program has supported DARPA's PACT program. The goal of the PHAST program was to develop a 10-bit, 10-Gsps analog-to-digital converter (ADC). This objective was to be accomplished in two phases; Phase I with a goal of delivering an 8-bit, 10-Gsps prototype system, and Phase II, which would focus on developing a 10-bit, 10-Gsps brassboard system. Early in Phase I, a 4-bit ADC was fabricated and successfully tested. The 8-bit ADC required development of a high-speed tunable laser, which was designed and in the process of fabrication when we were redirected to stop work on the project. The existing design described in this document would have been used as the template to fabricate the Phase I prototype. We believe that the innovative high-speed tunable laser that was under development at the time we were redirected to stop work could have been successfully fabricated and would have served as an essential component in the high-speed ADC system and would have had many other useful applications in WDM and other areas.

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